RAMAIAH
Institute of Technology

CURRICULUM

(Effective from the Academic Year 2024 – 2025)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

I - IV SEMESTER M. Tech
(VLSI Design and Embedded Systems)

RAMAIAH INSTITUTE OF TECHNOLOGY
(Autonomous Institute, Affiliated to VTU)
(Approved by AICTE, New Delhi & Govt. of Karnataka)
Accredited by NBA & NAAC with A^+ Grade

About the Institute

In 1962, Dr. M. S. Ramaiah, a visionary philanthropist, established the Gokula Education Foundation with a noble mission to uplift society through education. The same year marked a pivotal moment in technical education in India with the founding of the M S Ramaiah Institute of Technology (MSRIT).

MSRIT offers an impressive array of 18 undergraduate and 15 postgraduate programs, all approved by the All India Council for Technical Education (AICTE). The National Board of Accreditation (NBA) has accredited all eligible programs at the undergraduate (UG) and postgraduate (PG) levels. In March 2021, MSRIT earned an 'A^{+}' grade from the National Assessment and Accreditation Council (NAAC), underscoring its unwavering commitment to academic excellence. Since 2007, the institute has proudly held Autonomous Status for its UG and PG programs, a prestigious recognition granted by the University Grants Commission (UGC) and Visvesvaraya Technological University (VTU). According to the Ministry of Education, Government of India's NIRF Ranking Framework, MSRIT ranks 75th among 1,584 leading engineering institutions and 31st among 131 architecture schools in India for 2025, highlighting its remarkable impact and leadership in education.

The institute participated in the Technical Education Quality Improvement Program (TEQIP), an initiative of the Government of India. To foster a research culture, the institute has established several specialized centres, including the Centre for Imaging Technologies, the Centre for Advanced Materials Technology, the Centre for Antennas and Radio Frequency Systems (CARFS), the Centre for Cyber Physical Systems, the Schneider Centre of Excellence, the Centre for Bio and Energy Materials Innovation, JSW Centre of Excellence in Power Systems and more. MSRIT boasts a faculty of 380 highly qualified members, 70% of whom hold doctoral degrees, and over 300 scholars currently pursuing Ph.D. degrees.

The Entrepreneurship Development Cell (EDC) and "Ramaiah Evolute" have been established on campus to support startup incubation. MSRIT features a dedicated Placement and Training department, a strong mentoring and proctorial system, a fully equipped sports department, and a spacious, air-conditioned library with a wide range of books and subscriptions to both international and national journals. The Digital Library provides access to online e-journals from renowned publishers, including Elsevier ScienceDirect, IEEE, Taylor & Francis, and SpringerLink. Additionally, the Institute is a member of DELNET, CMTI, and the VTU E- Library Consortium.

The institute features a state-of-the-art auditorium, a well-equipped recording studio, and multiple advanced conference halls with videoconferencing capabilities. Additionally, MSRIT provides excellent hostel accommodations for both boys and girls, ensuring a comfortable living environment. MSRIT alumni have achieved remarkable success, holding prominent positions in India and internationally. They maintain strong connections with the institute through an engaged and active Alumni Association.

Founded on Dr. Ramaiah's unwavering commitment to knowledge and innovation, this remarkable institution continues to inspire generations of students and shape the future of engineering and technology in the country.

About the Department

The Department of Electronics and Communication was started in 1975 and has grown over the years in terms of stature and infrastructure. The department has well equipped simulation and electronic laboratories and is recognized as a research center under VTU. The department currently offers a B. E. program with an intake of 120, and two M. Tech programs, one in Digital Electronics and Communication, and one in VLSI Design and Embedded Systems, with intakes of 30 and 18 respectively. The department has a Center of Excellence in Food Technologies sponsored by VGST, Government of Karnataka. The department is equipped with numerous UG and PG labs, along with R & D facilities. Past and current research sponsoring agencies include DST, VTU, VGST and AICTE with funding amount worth Rs. 1 crore. The department has modern research ambitions to develop innovative solutions and products and to pursue various research activities focused towards national development in various advanced fields such as Signal Processing, Embedded Systems, Cognitive Sensors and RF Technology, Software Development and Mobile Technology.

VISION OF THE INSTITUTE

To be an Institution of International Eminence, renowned for imparting quality technical education, cutting edge research and innovation to meet global socio-economic needs

MISSION OF THE INSTITUTE

RIT shall meet the global socio-economic needs through

- Imparting quality technical education by nurturing a conducive learning environment through continuous improvement and customization
- Establishing research clusters in emerging areas in collaboration with globally reputed organizations
- Establishing innovative skills development, techno-entrepreneurial activities and consultancy for socio-economic needs

QUALITY POLICY

We at M. S. Ramaiah Institute of Technology strive to deliver comprehensive, continually enhanced, global quality technical and management education through an established Quality Management System complemented by the synergistic interaction of the stake holders concerned

VISION OF THE DEPARTMENT

To evolve into a department of national and international repute for excellence in education and cutting-edge research in the domain of Electronics and Communication Engineering

MISSION OF THE DEPARTMENT

The department will continuously strive to

1. Provide a world-class learning environment that caters to local and global technological and social requirements
2. Initiate research collaborations with academia and industries to perform cutting edge research leading to socio-technological innovations
3. Develop skills for pursuing innovation and entrepreneurial ventures for graduating engineers

PROGRAM EDUCATIONAL OBJECTIVES (PEOs):

PEO1: Be successful practicing professionals or pursue doctoral studies in areas related to VLSI Design & Embedded Systems, contributing significantly to research and development activities

PEO2: Engage in professional development in the area of VLSI Design & Embedded Systems by adapting to new technology and career challenges

PEO3: Demonstrate professional, ethical, and social responsibilities of the VLSI Design & Embedded Systems Professionals

PROGRAM OUTCOMES (POs):

PO1: Development of Solutions: An ability to independently carry out research/investigation and development work to solve practical problems

PO2: Technical Presentation Skills: An ability to write and present a substantial technical report/document

PO3: Analyze Complex Systems: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: Develop Novel Designs: An ability to apply their in-depth knowledge in the VLSI Design & Embedded Systems domain to evaluate, analyze and synthesize existing and novel designs

PO5: Modern Tools Usage: An ability to apply appropriate techniques and modern tools in design and implementation of system in the domain of VLSI Design & Embedded Systems

CURRICULUM CREDITS DISTRIBUTION

Semester	Professional Core Course (PCC)	Professional Core Course Lab (PCCL)	Professional Elective Course (PEC)	Mandatory Credit Course (MCC)	Project Work / Seminar (PW)	Internship (INT)	Total semester credits
First	6	2	11	3	-	-	22
Second	8	2	12	-	-	-	22
Third	4	-	4	-	4	4	16
Fourth	-	-	-	-	20	--	20
Total	**18**	**4**	**27**	3	**24**	**4**	**80**

SCHEME OF TEACHING

M. Tech (VLSI Design and Embedded Systems)

I SEMESTER

S. No	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MVE11	Advanced Engineering Mathematics	PS-C	2	1	0	3	4
2.	MVE12	Digital System Design using HDL	PS-C	3	0	0	3	3
3.	MVEExx	Elective 1	PS-E	4	0	0	4	4
4.	MVEExx	Elective 2	PS-E	4	0	0	4	4
5.	MVEExx	Elective 3	PS-E	3	0	0	3	3
6.	RM116	Research Methodology and IPR		3	0	0	3	3
7.	MVEL13	Digital System Design Laboratory	PS-C	0	0	1	1	2
8.	MVEL14	Advanced Embedded Systems Laboratory	PS-C	0	0	1	1	2
Total				**19**	**1**	**2**	**22**	**25**

II SEMESTER

S. No	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MVE21	Analog and Mixed Signal IC Design	PS-C	3	1	0	4	4
2.	MVE22	ARM System Design	PS-C	4	0	0	4	4
3.	MVEExx	Elective 4	PS-E	4	0	0	4	4
4.	MVEExx	Elective 5	PS-E	4	0	0	4	4
5.	MVEExx	Elective 6	PS-E	4	0	0	4	4
6.	MVEL23	Analog and Mixed Signal IC Design Laboratory	PS-C	0	0	1	1	2
7.	MVEL24	Advanced Microcontroller Laboratory	PS-C	0	0	1	1	2
Total				**19**	**1**	**2**	**22**	**24**

III SEMESTER

S. No	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MVE31	SoC Design	PS-C	3	1	0	4	4
2.	MVEExx	Elective 7	PS-E	4	0	0	4	4
3.	MVE32	Internship/Industrial Training	IN	0	0	4	4	8
4.	MVE33	Project Work – I	PW	0	0	4	4	8
Total				**7**	**1**	**8**	**16**	**24**

IV SEMESTER

S. No	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MVE41	Project Work – II	PW	0	0	20	20	40
Total				**0**	**0**	**20**	**20**	**40**

List of Electives

S. No	Course Code	Course Name	Credits			
			L	T	P	Total
1.	MVEE01	Advanced Embedded Systems	4	0	0	4
2.	MVEE02	VLSI Circuits and System	4	0	0	4
3.	MVEE03	Digital VLSI Testing	3	0	0	3
4.	MVEE04	Advanced Digital Logic Verification	4	0	0	4
5.	MVEE05	Embedded Linux	4	0	0	4
6.	MVEE06	Machine Learning and Deep Learning	4	0	0	4
7.	MVEE07	Internet of Things (IoT)	4	0	0	4
8.	MVEE08	Physics of Semiconductor Devices	4	0	0	4
9.	MVEE09	ASIC Design	4	0	0	4
10.	MVEE10	Physical VLSI Design	4	0	0	4
11.	MVEE11	Low Power VLSI Design	4	0	0	4

ADVANCED ENGINEERING MATHEMATICS	
Course Code: MVE11	**Credits: 2:1:0**
Prerequisite: Engineering Mathematics	**Contact Hours: 28L+14T**
Course Coordinator: M. Girinath Reddy	

Course Contents

Unit I

Linear Algebra I: Geometry of linear equations, Solution sets of linear systems, Gaussian elimination method, Gauss Seidel method, Matrix notation, inverses, Partitioned matrices, Matrix factorization and determinants.

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit II

Linear Algebra II: Linear transformations, Composition of matrix transformations, Rotation about the origin, Dilation, Contraction and Reflection, Vector spaces and subspaces, linear independence, rank, basis and dimension, linear transformation, change of basis.

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit III

Graph Theory: Introduction, Isomorphism, Connected Graphs, Disconnected Graphs, Trees, Cut-sets, Vector spaces of Graphs, Electrical network analysis by graph theory

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit IV

Linear Differential Equations: Definitions, completer solutions, rules for finding the complementary function, inverse operator, rules for finding the particular integral, Cauchy's and Legendre's linear equations, linear dependence of solutions, simultaneous linear equations with constant coefficients

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit V

Partial Differential Equations: Introduction, formation of partial differential equations, solutions of partial differential equations, homogeneous linear equations with constant coefficients, working procedure to solve homogeneous linear equations, rules for finding complementary function, non-homogeneous linear equation.

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Reference Books:

1. Gareth Williams, "Linear Algebra with Applications", 6th Edition, Jones and Barlett Publishers, 2011
2. David C Lay, "Linear Algebra and its Applications", 3rd Edition, Pearson Education, 2013
3. Narsingh Deo, "Graph Theory with Applications to Engineering and Computer Science", PHI Learning, 2011
4. M. P. Deisenroth, A. A. Faisal, C. S. Ong, "Mathematics for Machine Learning", 1st Edition, Cambridge University Press, 2020.
5. B.S. Grewal, "Higher Engineering Mathematics", 44th Edition, Khanna Publication, 2018

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Solve linear equations using Gauss elimination and Gauss Seidel methods (POs: 1, 3, 4, 5)
2. Verify if the given set forms a basis of a vector space and change the bases in the vector space (POs: 1, 3, 4, 5)
3. Use graph theoretic idea for electrical network analysis (POs: 1, 3, 4, 5)
4. Use analytical methods to solve higher order ordinary differential equations and simultaneous differential equations a raising in many practical applications (POs: 1, 3, 4, 5)
5. Learnt to form and solve PDE's for homogeneous and non-homogenous and linear equations (POs: 1, 3, 4, 5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

DIGITAL SYSTEM DESIGN USING HDL	
Course Code: MVE12	**Credits: 3:0:0**
Prerequisite: Digital Design	**Contact Hours: 42L**
Course Coordinator: Dr. Rajendra Prasad P	

Course Contents

Unit I

Introduction and Methodology: Digital systems and embedded systems, Binary representation and circuit elements, Real world circuits, Models, Design methodology

Number Basics: Unsigned and signed integers, Fixed and floating point numbers

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117108040
- Links: https://nptel.ac.in/courses/117105080

Unit II

Sequential Basics: Storage elements, Counters, Sequential data paths and control, Clocked synchronous timing methodology

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117106092
- Links: https://nptel.ac.in/courses/117106086

Unit III

Memories and Implementation Fabrics: Concepts, Memory types, Error detection and correction, ICs, PLDs, Packaging and circuit boards, Interconnection and signal integrity

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117106109
- Links: https://nptel.ac.in/courses/117106114

Unit IV

System Verilog Simulation and Synthesis: System Verilog extension to Verilog, RTL and gate level modeling, RTL synthesis, Subset of System Verilog, System Verilog simulation, Digital synthesis, Modules, Procedural blocks

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/108103179
- Links: https://nptel.ac.in/courses/106105165

Unit V

RTL Modeling Fundamentals: System Verilog language rules – Module, Module instances, Hierarchy, Four state data values, Data types, Variable types, Net types, Operators, Continuous signal assignments, Procedural signal assignments, Modeling combinational logic and sequential logic

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106105165
- Links: https://nptel.ac.in/courses/108103179

Reference Books:

1. Peter J. Ashenden, "Digital Design: An Embedded Systems Approach using Verilog", Elsevier, 2010.
2. Stuart Sutherland, "RTL Modeling with System Verilog for Simulation and Synthesis: Using System Verilog for ASIC and FPGA Design", 1st Edition, Create Space Independent Publishing Platform, 2017.
3. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", 2nd Edition, Pearson Education, 2010.
4. Chris Spear, Greogory J Tumbush, "System Verilog for Verification – A Guide to Learning Test Bench Language Features", Springer, 2012.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Apply the concepts of Verilog modeling to design and verify the operations of complex digital logic circuits. (POs: 1, 3, 4,5)
2. Design and test pipelined storage elements, sequential data path controllers using, Verilog. (POs:.1,3,4,5)
3. Apply concept of Verilog modeling to multi-port memories, FIFO data paths and FSMs with respect to integrated circuits. (POs: 1, 3, 4,5)
4. Employ System Verilog to simulate and synthesize digital systems. (POs: 1,3,4,5)
5. Model combinational and sequential circuits using System Verilog. (POs: 1, 3, 4,5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

RESEARCH METHODOLOGY & IPR	
Course Code: MVE12	**Credits: 3:0:0**
Prerequisite: Nil	**Contact Hours: 42L**
Course Coordinator: Dr. Shilpa M	

Course Contents

Unit I

Research Methodology: Introduction, Meaning of research, Objectives of research, Motivation in research, Types of research, Research approaches, Significance of research, Research methods versus methodology, Research and scientific method, Importance of knowing how research is done, Research process, Criteria of good research, Problems encountered by researchers in India.

Defining the Research Problem: What is research problem, Selecting the problem, Necessity of defining the problem, Technique involved in defining a problem, An illustration.

- Pedagogy/Course delivery tools: Chalk, power point presentations and talk
- Links: https://archive.nptel.ac.in/courses/110/105/110105139/

Unit II

Literature review: Primary and secondary sources, Reviews, Monograph, Patents, Research databases, Web as a source, Searching the web, Critical literature review, Identifying gap areas from literature and research database, Development of working hypothesis.

Research Design: Meaning of research design, Need for research design, Features of a good design, Important concepts relating to research design, Different research designs, Basic principles of experimental design.

- Pedagogy/Course delivery tools: Chalk, power point presentations and talk
- Links: https://archive.nptel.ac.in/courses/110/105/110105139/

Unit III

Sampling Design: Census and sampling survey, Implications of a sample design, Steps in sampling design, Criteria of selecting a sampling procedure, Characteristics of a good sample design, Different types of sample designs, How to select a random sample, Random sample from an infinite universe, Complex random sampling designs.

Methods of Data Collection: Collection of primary data, Observation method, Interview method, Collection of data through questionnaires, Collection of data through schedules, Different between questionnaires and schedules, some other methods of data collection, Collection of secondary data, Selection of appropriate method for data collection, Case study method.

- Pedagogy/Course delivery tools: Chalk, power point presentations and talk
- Links: https://archive.nptel.ac.in/courses/110/105/110105139/

Unit IV

Multivariate Analysis: The nature of multivariate analysis, Classifying multivariate techniques, Analysis of dependence, Analysis of interdependence.

Probability distributions: Introduction to Probability, Laws of Probability, Baye's theorem, Discrete and Continuous random variables, Binomial, Poisson distributions, Normal and Exponential distributions - Simple problems, applications**.**

- Pedagogy/Course delivery tools: Chalk, power point presentations and talk
- Links: https://archive.nptel.ac.in/courses/110/105/110105139/

Unit V

Research Ethics and Intellectual Property: Ethics- Ethical issues, Ethical committees (human & animal), Research ethics; IPR- Intellectual property rights and Patent law, Commercialization, Copyright, Royalty, Trade related aspects of intellectual property rights (TRIPS); Scholarly publishing- IMRAD concept and design of research paper, Citation and acknowledgement, Plagiarism, Reproducibility and Accountability.

- Pedagogy/Course delivery tools: Chalk, power point presentations and talk
- Links: https://archive.nptel.ac.in/courses/110/105/110105139/

Text Books:

1. Kothari CR and Garg G. 2019. Research Methodology: Methods and Techniques, Fourth Edition, New Age International Publishers, ISBN: 978-81-224-2488-1.
2. Panneerselvam R. 2013. Research Methodology, Second Edition, Prentice Hall India Learning Private Limited, ISBN: 978-81-203-4946-9.

Reference Books:

1. Zikmund WG, Babin BJ, Carr JC and Griffin M. 2013. Business Research Methods, Ninth Edition, Cengage India Private Limited, ISBN: 978-93-535-0326-0.
2. Wadhera BL. 2010. Law Relating to Intellectual Property: Patent, Trademarks, Designs and Geographical Indication, Universal Law Publishing, ISBN: 978-93-503-5030-0.

Course Outcomes (COs):

At the end of the course the student will be able to

1. Understand the research methodology and define the problem for research (POs: 1, 2, 3, 4, 5)
2. Conduct literature review and apply the principles of research design (POs: 1, 2)
3. Apply the knowledge of various sampling procedures and different methods of data collection in the research (POs: 1, 2)
4. Apply multi-variate techniques and concepts of probability distributions to real-time situations (POs: 1, 2, 3)
5. Apply ethics and concepts of intellectual property in the research process (POs: 1, 2, 3, 4)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course out comes addressed**
Internal test-I	30	CO1,CO2
Internal test-II	30	CO3,CO4,CO5
Average of the two internal tests shall be taken for30marks.		
Other components		
Quiz/ Presentations	10	CO1,CO2
Assignment	10	CO3,CO4,CO5
Semester End Examination (SEE):	100	CO1,CO2,CO3,CO4,CO5

DIGITAL SYSTEM DESIGN LABORATORY	
Course Code: MVEL13	**Credits: 0:0:1**
Prerequisite: Digital Electronics	**Contact Hours: 14P**
Course Coordinator: Dr. Rajendra Prasad P	

Course Contents

List of Experiments:

Using Verilog code design, simulate and synthesize the following with a suitable FPGA

1. 8 to 3 programmable priority encoder
2. Full Adder using structural modeling
3. Flip Flops(D,SR,T,JK)
4. 4-bit arbitrary counter,4-bit binary up/down/up-down counter with synchronous reset, 4-bit Johnson counter, BCD counter
5. Sequential block to detect a sequence (say 11101) using appropriate FSM
6. 8-bit ripple carry adder and carry skip adder
7. 8-bit carry select adder
8. Stepper motor and DC motor interface
9. DAC interface

Using System Verilog code, simulate the following

10. Full subtractor using structural modeling
11. Flip Flops(D,SR,T,JK)
12. 4-bit synchronous/asynchronous counters, synchronous arbitrary counter

References:

1. Peter J. Ashenden, "Digital Design: An Embedded Systems Approach using Verilog", Elsevier, 2010.
2. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", 2nd Edition, Pearson Education, 2010.
3. Stuart Sutherland, "RTL Modeling with System Verilog for Simulation and Synthesis: using System Verilog for ASIC and FPGA Design", 1st Edition, Create Space Independent Publishing Platform, 2017.

Web links and Video Lectures (e-Resources):

1. https://nptel.ac.in/courses/108105113
2. https://nptel.ac.in/courses/117103064
3. https://nptel.ac.in/courses/117106086
4. https://nptel.ac.in/courses/117106114
5. https://nptel.ac.in/courses/106105165
6. https://nptel.ac.in/courses/108103179

Course Outcomes (COs):

1. Design and model complex combinational circuits using HDL at behavioral, structural and RTL levels. (POs: 1, 3, 4, 5)
2. Enumerate complex sequential circuits using HDL at behavioral, structural and RTL levels. (POs: 1, 3, 4, 5)
3. Develop test benches to simulate combinational and sequential circuits. (POs: 1, 3, 4, 5)
4. Illustrate how the language infers hardware and helps to simulate and synthesize the digital system. (POs: 1, 3, 4, 5)
5. Implement and analyze the digital systems using FPGAs with respect to speed and area. (POs: 1, 3, 4, 5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Weekly evaluation of laboratory manuals/records after the conduction of every experiment	30	CO1, CO2, CO3, CO4, CO5
Practical test	20	CO1, CO2, CO3, CO4, CO5
Semester End Examination (SEE):	50	CO1, CO2, CO3, CO4, CO5

ADVANCED EMBEDDED SYSTEMS LABORATORY	
Course Code: MVEL14	**Credits: 0:0:1**
Prerequisite: Microcontrolles / Embedded System Design	**Contact Hours: 14P**
Course Coordinator: Dr. Suma K V	

Course Contents

List of Experiments

PCB Designing

1. Generation of schematic, Bill of Materials and Net list
2. Generation of layout
3. Gerber file Generation and Online viewer

Unified Modeling Language (UML)

4. Model the static aspects of the system using Use Case Diagram in UML
5. Model the static aspects of the system using

   Basic Class Diagram and generate code in UML

   Optimized Class Diagram and generate code in UML
6. Model the elevator system using sequence diagram in UML

RTOS programs

7. Create a process using fork ( ) function call
8. Demonstrate the functionality of a 'Signal' when a delete key is pressed
9. Multithreading – One thread reads the input from the keyboard and another thread converts topper case. This is done until 'Stop' is pressed. Number of threads can be running sharingsame CPU.
10. Intertask communication using following techniques-
    - semaphore
    - pipes
    - FIFO
    - Message queue

References:

1. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, First Edition, Reprint 2014.
2. James K Peckol, "Embedded Systems – A Contemporary Design Tool", John Wiley, 2nd Edition 2008.

Web links and Video Lectures (e-Resources):

Course Outcomes (COs):

1. Generate the schematic, netlist, bill of materials and layout for a given circuit (POs- 2, 3,5)
2. Generate Gerber files for actual PCB fabrication (POs - 2, 3, 4,5)
3. Generate UML static diagrams for a given embedded application (POs – 1, 2, 3, 4, 5)
4. Generate UML dynamic diagrams for a given embedded application (POs – 1, 2, 3, 4, 5)
5. Implement the basic concepts of RTOS such as threads, processes, semaphore & mutex (POs – 2,3,4,5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Weekly evaluation of laboratory manuals/records after the conduction of every experiment	30	CO1, CO2, CO3, CO4, CO5
Practical test	20	CO1, CO2, CO3, CO4, CO5
Semester End Examination (SEE):	50	CO1, CO2, CO3, CO4, CO5

ANALOG AND MIXED SIGNAL IC DESIGN	
Course Code: MVE21	**Credits: 3:1:0**
Prerequisite: Analog Electronics	**Contact Hours: 42L+14T**
Course Coordinator: Dr. V. Anandi	

Course Contents

Unit I

Single Stage Amplifier: CS stage with resistance load, diode connected load, Current source load, active load, triode load, CS stage with source degeneration, Source follower, Common-gatestage, Cascode stage, Folded cascode.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117101105
- Links: https://archive.nptel.ac.in/courses/108106105/
- Links: https://nptel.ac.in/courses/117106030
- Links: https://a.impartus.com/ilc/#/course/1307788/1112

Unit II

Frequency Response of CS stage: General considerations, Miller effect, Association of poles with nodes, Frequency response of common source stage.

Differential Amplifiers and Current Mirrors: Basic differential pair, Common mode response, differential pair with MOS loads, Gilbertcell, Basic current mirror, Cascode current mirror.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117101105
- Links: https://archive.nptel.ac.in/courses/108106105/
- Links: https://nptel.ac.in/courses/117106030
- Links: https://a.impartus.com/ilc/#/course/1307788/1112

Unit III

Operational Amplifiers: One-stage opamp, Two-stage opamp, Gain boosting, output swing calculations, common-mode feedback, input range, limitations, slew rate, PSRR, Noise in opamp.

Stability and Frequency Compensation: General considerations, multi-pole systems, phase margin, basic frequency compensation.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117101105
- Links: https://archive.nptel.ac.in/courses/108106105/
- Links: https://nptel.ac.in/courses/117106030
- Links: https://a.impartus.com/ilc/#/course/1307788/1112

Unit IV

Bandgap References and Switched-Capacitor Circuits: General considerations, supply independent biasing, Temperature independent biasing, PTAT current generation, Constant Gm biasing, sampling switches, switched capacitor amplifiers**.**

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117101105
- Links: https://archive.nptel.ac.in/courses/108106105/
- Links: https://nptel.ac.in/courses/117106030
- Links: https://a.impartus.com/ilc/#/course/1307788/1112

Unit V

Data Converter Architecture: DAC and ADC specifications, Qualitative analysis of resistor string DAC, R-2R Ladder networks, current steering DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, IntegratingADC

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://a.impartus.com/ilc/#/course/1307788/1112

Reference Books:

1. Behzad Razavi,"Design of Analog CMOS Integrated Circuits",2nd Edition, Tata McGraw-Hill, 2018.
2. Phillip E Allen, Douglas R Holberg,"CMOS Analog Circuit Design", 2nd Edition Oxford University Press,2013.
3. R.JacobBaker,"CMOS Circuit Design, Layout, Simulation", 2nd Edition, Wiley publications, 2005.
4. B.Razavi,"Microelectronics", 1st Edition Tata Mc GrawHill, 2001.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Relate the concept of MOS devices to various MOS amplifier applications.(POs:1,3,4,5)
2. Apply the concept of differential amplifiers with MOS loads to estimate the frequency response of one stage opamp. (POs:1,3,4,5)
3. Apply the concept to amplifiers to construct one, two stage op-amp and analyze the frequency compensation, stability of an op-amp. (POs: 1,3,4,5)
4. Illustrate the concept of bandgap references and switched capacitor circuits. (POs:1,3,4)
5. Analyze different types of ADCs and DACs (POs:1,3,4,5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

ARM SYSTEM DESIGN	
Course Code: MVE22	**Credits: 4:0:0**
Prerequisite: Microcontrollers/ Embedded system design	**Contact Hours: 56L**
Course Coordinator: Dr. Suma K V	

Course Contents

Unit I

Introduction to ARM Cortex M Processors: What are ARM Cortex M Processors, advantages of the Cortex M Processors, applications of the ARM Cortex M processors

Technical overview: General information, Architecture – introduction, programmer's model, behavior of the application program status word, memory system, exceptions and interrupts, system control block, Debug

- Pedagogy/Course delivery tools: Power point presentation, Chalk and talk
- Links: https://nptel.ac.in/courses/106105193

Unit II

Instruction set: Moving data within the processor, memory access, arithmetic operations, logic operations, shift and rotate instructions, data conversion operations, bit field processing, compare and test, program flow control, saturation operations, exception-related instructions, sleep mode-related instructions, memory barrier instructions.

- Pedagogy/Course delivery tools: Power point presentation, Chalk and talk
- Links: https://developer.arm.com/documentation/ddi0439/b

Unit III

Low power and system control features: Low power designs, low power features – sleep modes, system control register, entering sleep mode, wake-up conditions, low power features using WFI &WFE instructions in programming, sleep-on-exit feature, SEVONPEND, sleep extension/wake-up delay, WIC, event communication interface, low power features using WFI &WFE instructions in programming.

Cortex M4 floating point unit: Overview, floating point register overview, fault status registers and fault address registers, CPACR register, floating point register bank, FPSCR, FPCCR, FPCAR, FPDSCR, media and floating point feature registers

- Pedagogy/Course delivery tools: Power point presentation, Chalk and talk
- Links: https://developer.arm.com/ip-products/processors/cortex-m /

Unit IV

Fault exceptions & fault handling: Causes of faults, enabling fault handlers, fault status registers and fault address registers, analyzing faults.

- Pedagogy/Course delivery tools: Power point presentation, Chalk and talk
- Links: https://www.arm.com/technologies/floating-point

Unit V

The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of files generated on cross-compilation, Disassembler/DE complier, Simulators Emulators and Debugging

- Pedagogy/Course delivery tools: Power point presentation, Chalk and talk
- Links: https://developer.arm.com/documentation/dui0497/a/the-cortex-m0-instruction-set

Reference Books:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M4", 3rd Edition, Newnes (Elsevier) Publications, 2014.
2. Shibu K. V, "Introduction to Embedded Systems", 2nd Edition, Tata McGraw Hill Education Private Ltd., 2009.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Familiarize with the technical overview and architecture of ARM Cortex M4 (POs: 3, 5)
2. Apply the technical knowledge of ARM Cortex M4 to build programs (POs: 1, 3, 4, 5)
3. Illustrate the importance of low power mode and floating point features of ARM Cortex M4 (POs: 1, 3, 4)
4. Identify the causes of failures in ARM Cortex M4 using fault exception mechanism (POs: 1, 4, 5)
5. Analyze the working of debugger tools for embedded system design and development (POs:1, 4, 5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

ANALOG AND MIXED SIGNAL IC DESIGN LABORATORY	
Course Code: MVEL23	**Credits: 0:0:1**
Prerequisite: Nil	**Contact Hours: 14P**
Course Coordinator: Dr. V. Anandi	

Course Contents

List of Experiments

1. Design the CMOS Inverter circuit for the given specifications and complete the design flow mentioned below: a) Draw the schematic and verify the following: DC Analysis, AC Analysis, Transient Analysis
2. Design the Common Source Amplifier circuit for the given specifications and complete the design flow mentioned below: a) Draw the schematic and verify the following: DC Analysis, AC Analysis
3. Design of Common Source Amplifier for transient analysis
4. Design the Common Drain Amplifier the for given specifications and complete the design flow mentioned below: a) Draw the schematic and verify the following: DC Analysis, AC Analysis, Transient Analysis
5. Design the Common Gate Amplifier the for given specifications and complete the design flow mentioned below: a) Draw the schematic and verify the following: DC Analysis, AC Analysis, Transient Analysis
6. Design the differential Amplifier the for given specifications and complete the design flow: i) Draw the schematic and verify the following: DC Analysis, AC Analysis,
7. Design of differential Amplifier for Transient Analysis i) calculate Bandwidth and CMRR
8. Design a single-stage op-amp for given specifications and complete the design flow mentioned below: a) Draw the schematic and verify the following: DC Analysis, AC Analysis
9. Design of single-stage op-amp for Transient Analysis b) calculation of Bandwidth
10. Design a two-stage op-amp with given specifications and complete the design flow mentioned below: a) Draw the schematic and verify the following: DC Analysis, AC Analysis, Transient Analysis b) calculate Bandwidth
11. Design a 4-bit R-2R DAC with the given and complete the design flow mentioned below: Draw the schematic and verify the following: DC Analysis, AC Analysis

References:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition Tata McGraw-Hill, 2018
2. Phillip E Allen, Douglas R Holberg, "CMOS Analog Circuit Design", Oxford University Press,2004.

Web links and Video Lectures (e-Resources):

1. http://vlabs.iitkgp.ernet.in/vlabs/vlab2/

Course Outcomes (COs):

At the end of the course, the student will be able to

1. Design and analyze the operation of current mirrors and single-stage amplifiers. (POs: 1, 3, 4, 5)
2. Analyse the frequency response of the different configurations of an amplifier. (POs: 1, 3, 4, 5)
3. Design and analyse frequency response characteristics of Differential Amplifier, OP-AMP. (POs: 1, 3, 4, 5)
4. Ability to understand stability compensation for amplifiers. (POs: 1, 3, 4, 5)
5. Demonstrate proficiency in using VLSI CAD tools for design and analysis of mixed-signal circuits. (POs: 1, 3, 4, 5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Weekly evaluation of laboratory manuals/records after the conduction of every experiment	30	CO1, CO2, CO3, CO4, CO5
CIE test	20	CO1, CO2, CO3, CO4, CO5
Semester End Examination (SEE):	50	CO1, CO2, CO3, CO4, CO5

ADVANCED MICROCONTROLLER LABORATORY	
Course Code: MVEL24	**Credits: 0:0:1**
Prerequisite: Nil	**Contact Hours: 14P**
Course Coordinator: Dr. Lakshmi Shrinivasan	

Course Contents

List of Experiments:

Assembly Language Coding:

1. Programs involving Data Transfer Instructions
2. Programs involving Arithmetic instructions
3. Programs involving logical instructions
4. Programs for Sorting and Finding largest element in an array
5. Programs for Code conversion between BCD, ASCII & Hexadecimal
6. Program for finding Factorial of a number
7. Programs using low power modes
8. Programs using interrupts

Peripheral interfacing using ARM Cortex M4:

9. Display (LCD & LED) modules
10. Generation of Sine & Square waveforms using Dual DAC
11. Elevator
12. Calculator-type keyboard
13. Relay output
14. Stepper Motor

References:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M4", 3rd Edition, Newnes (Elsevier) Publication, 2014.

Web links and Video Lectures (e-Resources):

Course Outcomes (COs):

1. Employ simulation and emulation IDE for implementation (POs: 4, 5)
2. Write, compile and debug assembly language and C programs for ARM Cortex M4 (POs: 1, 3, 5)
3. Write C language programs to interface display modules and data converters to ARM Cortex M4 (POs: 1, 4, 5)
4. Write C language programs to control DC motor, stepper motor and relay through ARM Cortex M4 (POs: 1, 4, 5)
5. Write C language programs to interface keyboard, RTC and temperature sensor modules to ARM Cortex M4 (POs: 1, 4, 5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Weekly evaluation of laboratory manuals/records after the conduction of every experiment	30	CO1, CO2, CO3, CO4, CO5
CIE test	20	CO1, CO2, CO3, CO4, CO5
Semester End Examination (SEE):	50	CO1, CO2, CO3, CO4, CO5

SOC DESIGN LABORATORY	
Course Code: MVE31	**Credits: 3:1:0**
Prerequisite: Nil	**Contact Hours: 42L+14T**
Course Coordinator: Dr. V. Anandi	

Course Contents

Unit I

Evaluation of SOC: Evaluation of silicon process Technology, The Evolution of Design Methodology, SOC Design, Comparison between System-on-Board, System-on-Chip, and System-in-Package, Motivation for SOC Design, Review of Moore's law. Introduction to the systems approach: system architecture: an overview,

Components of the System: processors, memories, and interconnects, hardware and software: programmability, versus performance, processor architectures, system - level interconnection, bus – based approach, network - on - chip approach, an approach for SoC design

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://www.arm.com/resources/education/onlinecourses/introduction-to-soc

Unit II

Chip Basics: Time, Area, Power, Reliability, and Configurability. introduction, design trade –offs, five big issues in system - on - chip (SoC) design, cycle time, the pipelined processor, defining a cycle, optimum pipeline, performance, die area and cost, processor area, ideal and practical scaling, power, area – time – power trade - offs in processor design, workstation processor, embedded processor.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://www.arm.com/resources/education/onlinecourses/introduction-to-soc

Unit III

Processors: processor selection for SoC: overview, examples: processor core selection, basic concepts in processor architecture, basic concepts in processor microarchitecture, buffers: minimizing pipeline delays,

Robust processors: vector, very long instruction word (VLIW), and superscalar, vector processors

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://www.arm.com/resources/education/onlinecourses/introduction-to-soc

Unit IV

Memory Design: System - on – chip and board - based systems, introduction, SoC external memory: flash, SoC internal memory: placement, the size of memory, scratchpads and cache memory, basic notions, cache organization, multilevel caches, SoC (on - die) memory systems, board - based (off - die) memory systems, simple dram and the memory array, SDRAM and DDR SDRAM

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://www.arm.com/resources/education/onlinecourses/introduction-to-soc

Unit V

Interconnect: Introduction, overview: interconnect architectures, what is an NOC? bus: basic architecture, arbitration and protocols, bus bridge, physical bus structure, bus varieties, SoC standard buses, AMBA, core connect, bus interface units: bus sockets and bus wrappers, analytic bus models, contention and shared bus,

Beyond the bus: NOC with switch interconnects, soc interconnect switches, static networks, dynamic networks, NOC layered architecture, bus versus NOC, static versus dynamic networks.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://www.arm.com/resources/education/onlinecourses/introduction-to-soc

Reference Books:

1. R.E. Michael J.Flynn, Wayne Luk, "Computer system Design: Systemon-Chip", Wiley-India, 2012.
2. Sudeep Pasricha, Nikil Dutt, "On Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.
3. Lin, Y-L.S. (ed.), "Essential issues in SOC design: designing complex systems-on-chip. Springer, 2006.
4. Wayne Wolf, "Modern VLSI Design: IP Based Design", Prentice-Hall India, Fourth edition, 2009.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Identify the applications of SOC in today's electronics industry. (PO-1, 3,4)
2. Identify the building blocks of commercially available system on board, system on chip, and system in package. (PO-1, 3,4, 5)
3. Provide the overview of embedded processors with different architectures (PO-1, 3,4)
4. Understand the concepts behind embedded memories with scratchpad and cache. (PO-1, 3,4, 5)
5. Describe the AMBA, NOC architectures and iidentify the usage in real time. (PO-1, 3,4, 5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

INTERNSHIP/INDUSTRIAL TRAINING	
Course Code: MVE32	**Credits: 0:0:4**
Prerequisite: Nil	**Contact Hours:**
Course Coordinator:	

Course Contents

The evaluation of students will be based on an intermediate presentation, along with responses to a questionnaire testing for outcomes attained at the end of the internship. The rubrics for evaluation of the presentation and the questionnaire for the report will be distributed at the beginning of the internship.

EVALUATION RUBRICS

Criteria	Max. Marks	Achievement Levels				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Complex Technical Blocks	**10**	No working knowledge of the domain.	Working knowledge of the domain, with some knowledge of internal details.	Detailed understanding of the system, along with underlying mechanisms.		**CO1**
Error Debugging	**10**	No ability to diagnose or correct errors, or improve performance.	An ability to diagnose errors, but not correct them, no intuition on improving performance.	Diagnose and correct erroneous system operation, and propose methods to improve system performance.		**CO2**
Professional and Ethical Behavior	**10**	No knowledge of the requirement of professional and ethical behavior.	Understands the requirement for professional and ethical behavior.	Can predict the effects of non-professional an un-ethical behavior in the workplace.		**CO3**
Engineering and Finance	**10**	Cannot make the connection between engineering decisions and their economic impact.	Predict the cost of engineering decisions.	Creates designs keeping their economic impact in mind.		**CO4**
Lifelong Learning	**10**	No understanding of the requirements for lifelong learning in the engineering profession.	Can present examples of the impact of lifelong learning in the engineering industry.	Can present examples of the impact of lifelong learning, along with predicting future areas of impact of life-long learning.		**CO5**
TOTAL MARKS AWARDED						

Course Outcomes (COs):

1. Analyze the working of complex technical systems/blocks. (POs: 1, 2, 3, 4, 5)
2. Correct errors during functioning and improve the performance of complex technical systems/blocks. (POs: 1, 2, 3, 4, 5)
3. Understand the importance of professional and ethical behavior in the engineering workplace. (POs: 1, 2, 3, 4, 5)
4. Predict the effect of engineering decisions on financial matters. (POs: 1, 2, 3, 4, 5)
5. Appreciate the requirements for constant technology updation. (POs: 1, 2, 3, 4, 5)

PROJECT WORK – I	
Course Code: MVE33	**Credits: 0:0:4**
Prerequisite: Nil	**Contact Hours:**
Course Coordinator:	

Course Contents

The students will be evaluated based on two oral presentations during the semester. In the presentations they will have to discuss the results of their literature survey and initial implementations of the design.

EVALUATION RUBRICS

Criteria	Max. Marks	Achievement Levels				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Complex Technical Blocks	**10**	No working knowledge of the domain.	Working knowledge of the domain, with some knowledge of internal details.	Detailed understanding of the system, along with underlying mechanisms.		**CO1**
Error Debugging	**10**	No ability to diagnose or correct errors, or improve performance.	An ability to diagnose errors, but not correct them, no intuition on improving performance.	Diagnose and correct erroneous system operation, and propose methods to improve system performance.		**CO2**
Professional and Ethical Behavior	**10**	No knowledge of the requirement of professional and ethical behavior.	Understands the requirement for professional and ethical behavior.	Can predict the effects of non-professional an un-ethical behavior in the workplace.		**CO3**
Engineering and Finance	**10**	Cannot make the connection between engineering decisions and their economic impact.	Predict the cost of engineering decisions.	Creates designs keeping their economic impact in mind.		**CO4**
Lifelong Learning	**10**	No understanding of the requirements for lifelong learning in the engineering profession.	Can present examples of the impact of lifelong learning in the engineering industry.	Can present examples of the impact of lifelong learning, along with predicting future areas of impact of life-long learning.		**CO5**
TOTAL MARKS AWARDED						

EVALUATION RUBRICS

Criteria	Max. Marks	Achievement Levels Phase – I, Review – I				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Introduction	**5**	Introduction is not clear, or is not technically accurate.	Introduction is accurate, but no in-depth analysis of the domain.	Clear introduction to the domain, along with design decisions and their impacts.		**CO1**
Literature survey	**10**	Few sources of low quality, with no proper discussion of results.	Appropriate discussion of existing results, but quality of sources is low.	Comprehensive list of results presented from recent quality sources.		**CO2**
Methods comparison	**5**	Methods not explained and compared in terms of internal implementation details.	Advantages and disadvantages discussed, but not with reference to actual methods.	Detailed description of existing methods, along with their advantages and disadvantages.		**CO3**
				TOTAL MARKS AWARDED		

Criteria	Max. Marks	Achievement Levels Phase – I, Review – II				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Methods discussion	**10**	No implementation level discussion of methods used in literature.	Brief discussion of tools used and results obtained therein.	Detailed discussion of tools used and their impact on the quality of results obtained in literature sources.		**CO3**
Technical Block Diagrams & Initial Results	**10**	Block Diagram is not technically justified & initial results are not complete.	Justified block diagram and proper tools used to generate results but are not same as existing literature.	Detailed block diagram with use of suitable tools with appropriate results discussed.		**CO4**
Technical Report	**10**	Poorly written document without paper clarity.	Report includes figures/block diagram but lacks technical aspects/methodologies/approaches.	Report includes figures with clear description, graphical explanation. Document must include a draft of review article.		**CO5**
				TOTAL MARKS AWARDED		

Course Outcomes (COs):

1. Introduce the technical area chosen and demonstrate that the focus of the study is on a significant problem worth investigation. (POs: 1, 2, 3, 4, 5)
2. Discuss existing/standard solution strategies for the problem identified and its deficiency in the current scenario. (POs: 1, 2, 3, 4, 5)
3. Compare and contrast various research outcomes as part of a literature survey of quality published academic work. (POs: 1, 2, 3, 4, 5)
4. Implement technical block diagram with usage of modern tools to obtain appropriate initial results.
5. Prepare quality technical report which includes research review article.

PROJECT WORK – II	
Course Code: MVE41	**Credits: 0:0:20**
Prerequisite: Nil	**Contact Hours:**
Course Coordinator:	

Course Contents

The students will be evaluated based on two oral presentations, in which they will present their proposed solutions to the problem identified, and discuss the implementation details and results obtained.

EVALUATION RUBRICS

Criteria	Max. Marks	Achievement Levels Phase – II, Review – I				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Proposed Block Diagram	**10**	A discussion of methods for optimization is not based on technical arguments.	One or more block diagrams presented for optimization, but not justified with technical arguments.	One or more block diagrams presented for optimization, along with along with accurate technical arguments for justification.		**CO1**
Results	**10**	Results are not matching expectations, or are not complete.	Complete results generated, but not an improvement on existing metrics.	Complete results generated with an improvement over existing approaches due to proposed block diagram.		**CO2**
TOTAL MARKS AWARDED						

Criteria	Max. Marks	Achievement Levels Phase – II, Review – II				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Design of Experiments	**10**	Few experiments conducted, with no relation to problem domain.	Significant experiments conducted, but with no structure and relation to problem domain.	Significant experiments conducted, with all relevant parameters being tested in an orderly manner, and with relevance to hypothesis.		**CO3**
Experimental Results & Discussions	**10**	Results and Discussions are not well optimized & qualified.	Methods & its results are moderately discussed but not to the level of the proposed method.	Optimized results and detailed discussion with advantage & disadvantage of the proposed method.		**CO4**
Report Writing & Research Article	**10**	Poorly written document without proper organization.	Properly organized document but lack in depth explanation of individual modules of proposed work.	Well drafted documents with clear explanation & discussion of all aspects of the proposed work. Documents must include a technical article to be submitted to a conference/journal .		**CO5**
TOTAL MARKS AWARDED						

Course Outcomes (COs):

1. Present different methods for improving existing performance metrics with respect to existing literature, along with justified technical arguments. (POs: 1, 2, 3, 4, 5)
2. Implement solutions proposed using appropriate software tools. (POs: 1, 2, 3, 4, 5)
3. Compare implemented solutions and choose the best possible option based on factors such as societal impact, cost, speed, and practicality. (POs: 1, 2, 3, 4, 5)
4. Perform extensive experiments with detailed discussion qualifying the results of the proposed work. (POs: 1, 2, 3, 4, 5)
5. Prepare a comprehensive project report comprising of clear details of implementation & detailed experimental results with required discussion. (POs: 1, 2, 3, 4, 5)

ELECTIVES

ADVANCED EMBEDDED SYSTEMS	
Course Code: MVEE01	**Credits: 4:0:0**
Prerequisite: Nil	**Contact Hours: 56L**
Course Coordinator: Dr. Suma K V	

Course Contents

Unit I

Typical Embedded System: Core of the Embedded System, Memory, Sensors and Actuators, Embedded Firmware, Other System Components. Characteristics and Quality Attributes of Embedded Systems

- Pedagogy/Course delivery tools: Chalk and talk, Powerpoint presentation
- Links: https://nptel.ac.in/courses/106105193

Unit II

Embedded system design and development: System design and development, life-cycle models- the waterfall model, the V cycle model, the spiral model and rapid prototyping incremental, problem solving – five steps to design, the design process, identifying the requirements, formulating the requirements specifications, the system design specification, system specifications vs system requirements.

Hardware Software Co-Design and Program Modeling: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design.

- Pedagogy/Course delivery tools: Chalk and talk, Powerpoint presentation
- Links: https://nptel.ac.in/courses/106105182
- Links: https://archive.nptel.ac.in/courses/106/105/106105182/

Unit III

Embedded Hardware Design and Development: EDA Tools, How to Use EDA Tool, Schematic Design – Place wire, Bus, port, junction, creating part numbers, Design Rules check, Bill of materials, Net list creation, PCB Layout Design – Building blocks, Component placement, PCB track routing.

Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages

- Pedagogy/Course delivery tools: Chalk and talk, Powerpoint presentation
- Links: https://www.electronicsforu.com/buyers-guides/eda-tools-circuit-design
- Links: https://www.synopsys.com/glossary/what-is-electronic-design-automation.html

Unit IV

Software modeling: Introduction to UML, UML Diagrams, use cases, class diagrams, dynamic modeling with UML, Interaction diagrams, Sequence diagrams, Fork and Join, Branch and merge, Activity diagram, State chart diagrams, dynamic modeling with structural design methods.

- Pedagogy/Course delivery tools: Chalk and talk, Powerpoint presentation
- Links: http://www.digimat.in/nptel/courses/video/106105153/L51.html
- Links: https://nptel.ac.in/courses/106101235

Unit V

Real-Time Operating System (RTOS) based Embedded System Design: Operating System Basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Device Drivers, How to Choose an RTOS.

- Pedagogy/Course delivery tools: Chalk and talk, Powerpoint presentation
- Links: https://elearn.nptel.ac.in/shop/nptel/real-time-operating-system/
- Links: https://www.digimat.in/nptel/courses/video/106105172/L13.html

Reference Books:

1. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, First edition, reprint 2014.
2. James K Peckol, "Embedded Systems – A Contemporary Design Tool", John Wiley, 2nd Edition 2008.
3. David A Patterson, John L Hennessy "Computer Organization and Design- ARM Edition", 4th Edition, Morgan Kauffman Publishers Elsevier, 2010.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Identify the basic building blocks, characteristics and quality attributes of embedded systems (POs – 1, 4).
2. Analyze the complete life cycle of embedded system design and development (POs – 1, 2, 4, 5).
3. Design a printed circuit board for a given circuit by using the PCB design IDE (POs – 1, 2, 4, 5).
4. Interpret the various computational models of software in embedded system design (POs – 1, 2, 4).
5. Select the RTOS for real time embedded system design (POs - 1, 2, 4, 5).

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

COURSE DESIGN, DELIVERY AND ASSESSMENT	
Course Code: MVEE02	**Credits: 4:0:0**
Prerequisite: CMOS VLSI CIRCUITS	**Contact Hours: 56L**
Course Coordinator: Dr. Raghuram S	

Course Contents

Unit I

MOS Transistor Theory: n MOS/p MOS transistor, threshold voltage equation, MOS Current conduction, Non-ideal V-I Characteristics,

CMOS inverter: Voltage Transfer Characteristics, β ratio, noise margin

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106106089
- Links: https://nptel.ac.in/courses/117101004
- Links: https://vlsi-iitg.vlabs.ac.in/
- Links: http://vlabs.iitkgp.ac.in/tcad/exp8/

Unit II

Circuit Characterization and Performance Estimation: Delay Estimation – transient response, RC delay model, Elmore delay model, Linear delay model, Sizing with the method of logical effort

Power: Static Power Consumption, Dynamic Power Consumption

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106106089
- Links: https://nptel.ac.in/courses/117101004

Unit III

Combinational Circuit Design: Static CMOS, Ratioed circuits, CVSL, Dynamic Circuits, Pass transistor circuits. transmission gate

Sequential Circuit Design: Sequencing Static Circuits, Circuit Design of Latches and Flip Flops

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106106089
- Links: https://nptel.ac.in/courses/117101004

Unit IV

Data Path Sub System Design: Introduction, Addition – Carry lookahead, Carry Select, Tree Adders – Brent Kung, Kogge Stone, Multiplication: Carry-Save format, Booth Algorithm

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106106089
- Links: https://nptel.ac.in/courses/117101004

Unit V

Memory Subsystem Design: SRAM, DRAM, ROM, CAM, PLA

Special Purpose Subsystems: Packaging, Clock Distribution, I/O

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106106089
- Links: https://nptel.ac.in/courses/117101004

Reference Books:

1. Neil H E Weste, David Harris, "CMOS VLSI Design: A System Perspective", 4th Edition, Pearson Education, 2014.
2. Jan Rabaey, B. Nikolic, A. Chadrakasan," Digital Integrated Circuits: A Design Perspective", 2nd Edition, Pearson,2016
3. Wayne Wolf, "Modern VLSI Design: System on Silicon", 3rd Edition, PHI, 2008.
4. Douglas A Pucknell, Kamran Eshraghian, "Basic VLSI Design", 3rd Edition, PHI, 2009.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Analyse the theory behind CMOS digital circuits (POs:1, 3, 4, 5)
2. Employ different performance metrics to predict the performance of VLSI circuits. (POs:1, 3, 4, 5)
3. Apply digital design concepts to demonstrate different data path functions. (POs: 1, 3, 4, 5)
4. Design and analyze dynamic CMOS circuits. (POs: 1, 3, 4, 5)
5. Predict variations in clock signals, and design circuits to reduce the effects of variation. networks. (POs: 1, 3, 4, 5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

DIGITAL VLSI TESTING	
Course Code: MVEE03	**Credits: 3:0:0**
Prerequisite: CMOS VLSI Design	**Contact Hours: 42L**
Course Coordinator: Dr. Deepali Koppad	

Course Contents

Unit I

Introduction: Role of testing, Testing during the VLSI life cycle, Challenges in VLSI testing, test economics, Yield, Fault coverage

Fault Modeling: Various fault models, Single Stuck-at fault – fault equivalence, fault collapsing.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117105137
- Links: https://drive.google.com/file/d/1n6agUcye7HE1xPItwQ03wow0b3g6NloU/view

Unit II

Logic and Fault Simulation: Simulation Models, Algorithms for true value simulation, Algorithms for fault simulation, Statistical methods for fault simulation.

Testability Measures: Controllability and Observability, SCOAP Testability analysis

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117105137
- Links: https://drive.google.com/file/d/1n6agUcye7HE1xPItwQ03wow0b3g6NloU/view

Unit III

Combinational Circuit Test Generation: ATPG Algebras, Combinational ATPG Algorithms – D-Algorithm, PODEM, FAN.

DFT and Scan Design: Ad-Hoc DFT, Scan based design.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117105137
- Links: https://drive.google.com/file/d/1n6agUcye7HE1xPItwQ03wow0b3g6NloU/view

Unit IV

Sequential Circuit Test Generation: Time frame expansion method, Simulation-based sequential ATPG.

Logic BIST: Test pattern generation, output response analyzer, BIST architectures, Fault coverage enhancement.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117105137
- Links: https://drive.google.com/file/d/1n6agUcye7HE1xPItwQ03wow0b3g6NloU/view

Unit V

Boundary Scan: Introduction and motivation, TAP controller and port, SOC test problems.

Memory Test: Notation, Faults – Fault Manifestations, Failure Mechanisms, Memory Test Levels, March Test Notation, Fault Modeling – Diagnosis Versus Testing Needs, Reduced Functional Faults

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117105137
- Links: https://drive.google.com/file/d/1n6agUcye7HE1xPItwQ03wow0b3g6NloU/view

Reference Books:

1. Laung-Terng Wang, Cheng-Wen Wu andXiaoqing Wen, (Eds.), "VLSI Test Principles and Architectures: Design for Testability", Morgan Kaufmann Publishers, 2006.
2. Michael L. Bushnell, Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
3. Zainalabedin Navabi, "Digital System Test and Testable Design", Springer New York, NY, 2011
4. Parag K. Lala, "Digital Circuit Testing and Testability", Academic Press, 1997

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Create and manipulate fault models of VLSI circuits. (POs – 1, 3, 4)
2. Perform fault simulations, and predict testability measures of digital circuits. (POs – 1, 3, 4, 5)
3. Generate optimized test patterns for combinational and sequential logic circuits. (POs – 1, 3, 4, 5)
4. Design scan chains and BIST modules for digital designs. (POs – 1, 3, 4)
5. Employ boundary scan elements in design. (POs – 1, 3, 4)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

ADVANCED DIGITAL LOGIC VERIFICATION	
Course Code: MVEE04	**Credits: 4:0:0**
Prerequisite: Digital Design	**Contact Hours: 56L**
Course Coordinator: Dr. Deepali Koppad	

Course Contents

Unit I

Verification Concepts: Concepts of verification, Importance of verification, Stimulus vs Verification, Test bench generation, Functional verification approaches, Typical verification flow, **Stimulus generation, Direct testing, Coverage:** Code coverage and functional coverage, Coverage plan

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit II

System Verilog – Language Constructs: Data types: Two state data, Strings, Arrays: Queues, Dynamic and associative arrays, Structs, Enumerated types. Program blocks, modules, interfaces, Clocking ports, Mod ports

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit III

System Verilog – Classes and Randomization: SV classes, Language evolution, Classes and objects, Class variables and methods, Class instantiation, Inheritance and encapsulation, Polymorphism, Randomization: Directed vs Random testing, Randomization: Constraint driven randomization

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit IV

System Verilog – Assertions and Coverage: Assertions-Introduction to assertion based verification, Immediate and concurrent assertions, Coverage driven assertion: Motivation, types of coverage, Cover group, Cover point, Cross coverage, Concepts of binning and event sampling

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit V

Building Test Bench: Layered test bench architecture, Introduction to Universal Verification Methodology (UVM), Overview of UVM, Base classes and simulation phases in UVM and UVM macros, Unified messaging in UVM, UVM environment structure, Connecting DUTvirtual interface

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Reference Books:

1. Chris Spear, Greogory J Tumbush, "System Verilog for Verification – A Guide to Learning Test Bench Language Features", Springer, 2012.
2. SasanIman, "Step by Step Functional Verification with System Verilog and OVM", Hansen Brown Publishing, 2008.
3. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design – A Guide to using System Verilog for Hardware Design and Modeling", 2nd Edition, Springer Publications, 2006.
4. Janick Bergeron, "Writing Test Benches using System Verilog", Springer International Edition, 2009.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Discuss the principle and importance of verification. (POs: 1, 3, 4)
2. Apply OOPs concepts in System Verilog to verify a digital system. (POs: 1, 3, 4, 5)
3. Develop basic verification environment using System Verilog. (POs: 1, 3, 4, 5)
4. Create random stimulus and track functional coverage using System Verilog. (POs: 1, 3, 4, 5)
5. Illustrate the concepts of layered test bench architecture and its components. (POs: 1, 3, 4, 5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

EMBEDDED LINUX SYSTEM DEVELOPMENT	
Course Code: MVEE05	**Credits: 4:0:0**
Prerequisite: Operating System	**Contact Hours: 56L**
Course Coordinator: Dr. Lakshmi Shrinivasan	

Course Contents

Unit I

Introduction: History of Embedded Linux, Why Embedded Linux, Embedded Linux Versus Desktop Linux, Frequently Asked Questions, Embedded Linux Distributions, Porting Roadmap. **Getting Started**: Architecture of Embedded Linux, Linux Kernel Architecture, User Space, Linux Start-Up Sequence, GNU Cross Platform Tool chain

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Links: https://busybox.net/live_bbox/live_bbox.html
- Links: http://vlabs.iitkgp.ernet.in/rtes/index.html

Unit II

Board Support Package: Inserting BSP in Kernel Build Procedure, Memory Map, Interrupt Management, the PCI Subsystem, Timers, UART and Power Management

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Links: https://busybox.net/live_bbox/live_bbox.html
- Links: http://vlabs.iitkgp.ernet.in/rtes/index.html

Unit III

Embedded Storage: Flash Map, MTD—Memory Technology Device, MTD Architecture, Sample MTD Driver for NOR Flash, The Flash-Mapping Drivers, MTD Block and Character Devices, MTD utils Package, Embedded File Systems, Optimizing Storage Space, Tuning Kernel Memory.

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Links: https://busybox.net/live_bbox/live_bbox.html
- Links: http://vlabs.iitkgp.ernet.in/rtes/index.html

Unit IV

Embedded Drivers: Linux Serial Driver, Ethernet Driver, I2C Subsystem on Linux, USB Gadgets, Watchdog Timer and Kernel Modules.

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Links: https://busybox.net/live_bbox/live_bbox.html
- Links: http://vlabs.iitkgp.ernet.in/rtes/index.html

Unit V

Porting Applications: Architectural Comparison, Application Porting Roadmap, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Links: https://busybox.net/live_bbox/live_bbox.html
- Links: http://vlabs.iitkgp.ernet.in/rtes/index.html

Reference Books:

1. P.Raghvan, Amol Lad and Sriram Neelakandan, "Embedded Linux System Design And Development", 1st Edition, Auerbach Publications, September 2019.
2. Karim Yaghmour, Jon Masters, Gilad Ben-Yossef, and Philippe Gerum, "Building Embedded Linux Systems", 2nd edition, O'Reilly publications, 2008.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Understand the embedded Linux development environment. (POs –1, 5)
2. Appraise the need of BSP in an embedded system. (POs – 1, 3, 5)
3. Select appropriate Linux model for embedded storage devices. (POs – 1, 3, 4, 5)
4. Appreciate various embedded Linux drivers. (POs – 1, 2, 3, 5)
5. Acquire the knowledge of porting applications to embedded Linux from a traditional RTOS. (POs – 1,2, 3, 4, 5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz/ Seminar	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

MACHINE LEARNING AND DEEP LEARNING	
Course Code: MVEE06	**Credits: 4:0:0**
Prerequisite: Nil	**Contact Hours: 56L**
Course Coordinator: Dr. K. Indira	

Course Contents

Unit I

Introduction: What is machine learning, Example machine learning applications

Supervised Learning: Learning a class from examples, VC dimension, PAC learning, Noise, Learning multiple classes, Regression, Model selection and generalization

Bayesian Decision Theory: Classification, Losses and risks, Discriminant functions, Association rules

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://onlinecourses.nptel.ac.in/noc22_cs29/

Unit II

Parametric Methods: Maximum likelihood estimation, Evaluating an estimator, Bayes estimator, Parametric classification, Regression, Tuning model capacity

Dimensionality Reduction: Subset Selection, Principal Component Analysis (PCA), Linear Discriminant Analysis (LDA)

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://onlinecourses.nptel.ac.in/noc22_cs29/

Unit III

Unsupervised Learning: Clustering: k–Means clustering, EM algorithm, Hierarchical clustering,

Decision Trees: Univariate trees: Classification and regression trees

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://onlinecourses.nptel.ac.in/noc22_cs29/

Unit IV

Multilayer Perceptrons: Perceptron, Training a perceptron, Learning Boolean functions, Multilayer perceptrons, Backpropagation algorithm, learning hidden representation Autoencoders

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117105084
- Links: https://nptel.ac.in/courses/108108148

Unit V

Deep Learning: Train multiple hidden layers, Impreving training convergence, Regularization, convolutional layers, Tuning the network structure, Learning sequences, GAN.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117105084

Reference Books:

1. Ethem Alpaydin, "Introduction to Machine Learning", 4th Edition, PHI Learning Pvt. Ltd, 2020.
2. Ian Goodfellow, Yoshua Bengio, Aaron Courville, "Deep Learning", MIT Press, 2017.
3. Christopher Bishop, "Pattern Recognition and Machine Learning", CBS Publishers & Distributors, 2010.
4. Tom Mitchell, "Machine Learning", McGraw Hill, 1997.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Examine the concepts of various supervised learning algorithms and employ Bayesian learning for classification (POs – 1, 3, 4,5)
2. Evaluate parametric methods for classification and investigate various dimensionality reduction algorithms (POs –1, 3, 4,5)
3. Analyse unsupervised learning algorithms and decision tree (POs –1, 3, 4,5)
4. Appreciate the concepts of multilayer perceptrons (POs – 1, 3, 4,5)
5. Understand deep neural networks and demonstrate how convolutional networks can be mapped to practical applications (POs – 1, 3, 4,5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

INTERNET OF THINGS (IoT)	
Course Code: MVEE07	**Credits: 4:0:0**
Prerequisite: Nil	**Contact Hours: 56L**
Course Coordinator: Dr. Suma K V	

Course Contents

Unit I

Introduction & Concepts: Definition and Characteristics of IoT, Things in IoT, IoT Protocols, IoT Functional Blocks, IoT Communication Models, IoT Communication APIs, IoT Enabling Technologies, IoT levels and deployment templates, IoT and M2M, SDN and NFV for IoT

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit II

Developing Internet of Things: IoT Platform design methodology, Specifications: Requirements, Process, Domain, Information, Services, Level, Functional, Operational, Integration, Application Development

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit III

IoT Physical Devices and End Points: Basic building blocks of an IoT Device, Raspberry Pi, Linux on Raspberry Pi, Raspberry Pi Interfaces: Serial, SPI, I2C

Programming Raspberry Pi with Python: Controlling LED, Interfacing Switch, Interfacing Light Sensor

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit IV

Web Application Framework: Django, Web Services for IoT, SkyNet Messaging Platform,

Data Analytics for IoT: Apache: Hadoop, Oozie, Storm, Real-Time Data Analysis, Tools for IoT

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit V

IoT Case Studies: Home Automation: Smart Lighting, Home Intrusion Detection; Cities: Smart Parking Environment: Weather Monitoring System, Weather Reporting Bot, Air Pollution Monitoring, Forest Fire Detection; Agriculture – Smart Irrigation, IoT Printer.

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Reference Books:

1. Arshdeep Bahga, Vijay Madisetti, "Internet of Things: A Hands-on Approach", University Press, 2015.
2. Pethuru Raj, Anupama C Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases Description", Taylor & Francis, CRC Press, 2017.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Understand the building blocks of internet of things, characteristics and related communication protocols. (POs-1,3, 5)
2. Learn basics of design, integration and applications of IoT models. (POs-1,3, 5)
3. Acquire the knowledge of basic blocks of an IOT devices using Raspberry Pi. (POs-3, 5)
4. Understand cloud storage models and web services for IoT. (POs-3, 5)
5. Appraise with various case studies. (POs-1,3,4, 5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

PHYSICS OF SEMICONDUCTOR DEVICES	
Course Code: MVEE08	**Credits: 4:0:0**
Prerequisite: Nil	**Contact Hours: 56L**
Course Coordinator: Dr. Raghuram S	

Course Contents

Unit I

Energy Bands and Charge Carriers in Semiconductors: Bonding forces in solids, Energy bands, Metals, Semiconductors, Insulators, Electrons and Holes, Effective mass, Fermi Level, Electron and hole concentrations in equilibrium

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit II

Conductivity and Mobility: Effects of temperature and doping on mobility, Hall effect, Carrier lifetime, Direct and indirect recombination, Diffusion and drift of carriers, Continuity equation, Steady state carrier injection

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit III

PN Junctions: Contact potential, Fermi levels and space charge, Junction current, Carrier injection, Time variation of stored charge, Capacitance of PN junctions, Schottky barriers, Rectifying and ohmic contacts, Heterojunctions

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit IV

Bipolar Junction Transistors: Fundamental operation, Amplification, Terminal currents, Cutoff and saturation, Secondary effects, Gummel Poon model, Capacitance and charging time, Heterojunction bipolar transistors

- Pedagogy/Course delivery tools:
- Links:

Unit V

MOS Capacitor and Threshold Voltage: MOSFET: Output and transfer characteristics, Short channel I-V model, Control of threshold voltage, Substrate bias effect, Subthreshold characteristics, Equivalent circuit, Secondary effects, Advanced MOSFET structures

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

References:

1. Ben Streetman, Sanjay Bannerjee, "Solid State Electronic Devices", 7th Edition, Prentice Hall India, 2014.
2. Robert F Pierret, "Semiconductor Device Fundamentals", 2nd Edition, Addison Wesley, 1996.
3. Robert F Pierret, "Advanced Semiconductor Fundamentals", 2nd Edition, Prentice Hall, 1992.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Estimate carrier concentration in semiconductors, given the type and doping level of impurities. (POs: 1, 3, 4, 5)
2. Predict drift and diffusion carrier concentration in semiconductors. (POs: 1, 3, 4, 5)
3. Compute the current through a PN junction, under forward and reverse biased conditions. (POs: 1, 3, 4, 5)
4. Apply basic and advanced electronic concepts to derive models for current flow in a BJT transistor. (POs: 1, 3, 4, 5)
5. Employ electronic concepts to predict qualitative and quantitative operating conditions of MOS transistors. (POs: 1, 3, 4, 5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

ASIC DESIGN	
Course Code: MVEE09	**Credits: 4:0:0**
Prerequisite: Nil	**Contact Hours: 56L**
Course Coordinator: Dr. V. Anandi	

Course Contents

Unit I

Introduction to ASICs: Full custom, Semi-custom and programmable ASICs, ASIC design flow, **ASIC cell libraries CMOS Logic:** Datapath logic cells: Data path elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path operators, I/O cells

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit II

ASIC Library Design: Logical effort: Predicting delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages

Programmable ASIC Logic Cells: MUX as Boolean function generators, Actel ACT: ACT 1, ACT 2 and ACT3 logic modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit III

Programmable ASIC I/O Cells: Xilinx and Altera I/O Block

Low-level Design Entry: Schematic entry: Hierarchical design, Netlist screener

ASIC Construction: Physical Design, CAD Tools

Partitioning: Goals and objectives, Constructive partitioning, Iterative partitioning improvement, KL and look ahead algorithms

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit IV

Floor Planning: Goals and objectives, Floor planning tools, Channel definition, I/O and Power planning, Clock planning

Placement: Goals and objectives, Min-cut placement algorithm, Iterative placement improvement, Physical design flow

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit V

Routing: Global routing: Goals and objectives, Global routing methods, Back-annotation

Detailed Routing: Goals and objectives, Measurement of channel density, Left-Edge and Area routing algorithms. Special routing, Circuit extraction and DRC

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

References:

1. M J S Smith, "Application Specific Integrated Circuits", Pearson Education, 2003.
2. Jose E France, Yannis Tsividis, "Design of Analog – Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.
3. Malcolm R Haskard , Lan C May, "Analog VLSI Design – NMOS and CMOS", Prentice Hall, 1998.
4. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations", Springer, 2011.
5. Rakesh Chadha, J. Bhasker, "An ASIC Low Power Primer: Analysis, Techniques and Specification", Springer Publications, 2015.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Describe the concepts of ASIC design methodology, data path elements and FPGA architectures. (POs: 1, 3,4, 5)
2. Design data path elements for ASIC cell libraries and compute optimum path delay. (POs: 1, 3, 4, 5)
3. Employ industry synthesis tools to achieve desired objectives. (POs: 1, 3, 4, 5)
4. Design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain physical design flow. (POs: 1, 3, 4, 5)
5. Create floor plan including partition and routing using CAD algorithms. (POs: 1, 3, 4, 5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (SEE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

PHYSICAL VLSI DESIGN	
Course Code: MVEE10	**Credits: 4:0:0**
Prerequisite: Nil	**Contact Hours: 56L**
Course Coordinator: Dr. Raghuram S	

Course Contents

Unit I

Netlist Partition Algorithms: Introduction to electronic design automation, Algorithms and complexity, Graph theory terminology, Introduction to netlists and system partitioning

Partitioning Algorithms: Kernighan-Lin algorithm

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit II

Chip Planning: Introduction, Optimization goals in floor planning, Floor plan representations

Floor Planning Algorithms: Floor plan sizing, Cluster growth, Simulated annealing, Pin assignment

Power and Ground Routing: Design of power-ground distribution network, Mesh routing, Integrated floor planning algorithms

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit III

Global Placement and Routing: Introduction and objectives of placement, Global placement algorithms: min-cut placement, analytic placement, simulated annealing, Modern placement algorithms, Routing terminology and goals

Single-Net Routing: Rectilinear routing, Dijsktra's algorithm, A*, Full net routing and Rip-up and Re-route, Global routing in a connectivity graph, Modern global routing, Over the cell routing algorithms

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit IV

Detailed and Specialized Routing: Building the horizontal and vertical constraint graphs, Left-edge algorithm, Dog-legging, Switchbox routing, Introduction to area routing, NonManhattan routing, Routing in clock networks, clock-tree synthesis

- Pedagogy/Course delivery tools: Chalk and talk
- Links:

Unit V

Timing Closure: Introduction, Static timing analysis, Zero-slack algorithm, Timing driven placement, Timing driven routing, Physical synthesis, Performance driven design flow

- Pedagogy/Course delivery tools: Chalk and talk

- Links:

References:

1. Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, "VLSI Physical Design: From Graph Partitioning to Timing Closure", 1st Edition, Springer, 2011.
2. Sadiq M Sait, Habib Youssef, "VLSI Physical Design Automation", 1st Edition, World Scientific Publishing, 1995.
3. Navid A Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd Edition, Springer, 2005.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Employ basic partitioning algorithms to netlists. (POs: 1, 3, 4, 5)
2. Compute the area using different floor planning algorithms. (POs: 1, 3, 4, 5)
3. Predict the cost on the resultant wiring due to different place and route algorithms. (POs: 1, 3, 4, 5)
4. Apply routing algorithms to interconnect and clock networks. (POs: 1, 3, 4, 5)
5. Choose appropriate interconnections in the presence of timing constraints. (POs: 1, 3, 4, 5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

LOW POWER VLSI DESIGN	
Course Code: MVEE11	**Credits: 4:0:0**
Prerequisite: CMOS VLSI Design	**Contact Hours: 56L**
Course Coordinator: Pavitha U S	

Course Contents

Unit I

Power Dissipation in CMOS: Introduction: Need for low power VLSI chips, Sources of power consumption, Introduction to CMOS inverter power dissipation, Low power VLSI design limits, Basic principle of low power design.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://archive.nptel.ac.in/courses/106/105/106105034/#
- Links: https://drive.google.com/file/d/1LbYQNyw1oaAsU99YpGlh035tbtkd5f9S/view

Unit II

Logical Level Power Optimization: Gate reorganization, Local restructuring, Signal gating, Logic encoding, State machine encoding, Pre-computation logic.

Circuit Level Power Optimization: Transistor and gate sizing, Equivalent pin ordering, Network restructuring and re-organization, Special latches and flip-flops.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://drive.google.com/file/d/1RutCfSyV1K7Ln2J-TxILf3lOlhS3VhiZ/view
- Links:

Unit III

Low Voltage Low Power Adders: Standard adder cells, CMOS adder's architecture, Low voltage low power design techniques, Current mode adders

Special Techniques: Power reduction and clock networks, CMOS floating gate, Low power bus, Delay balancing.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://drive.google.com/file/d/1nEB6-KMX5OiwtQNbNG6xHpIT2IE6laT/view
- Links:

Unit IV

Low Voltage Low Power Multipliers: Overview of multiplication, Types of multiplier architectures, Braun multiplier, Baugh-Wooley multiplier, Booth multiplier, Wallace tree multiplier, Delay balancing in multipliers

Low Voltage Low Power Random Access Memories: Basics of SRAM and DRAM, Memory cell, Types of DRAM

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://drive.google.com/file/d/1W96DHjGQ0RNkMSJyaqu6vPBEC5twU3Rv/view

Unit V

Architecture and System: Power and performance management, Switching activity reduction, parallel architecture with voltage reduction, and flow graph transformation.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://archive.nptel.ac.in/courses/106/105/106105034/#
- Links: https://drive.google.com/file/d/14GPVPpyjozDMMXUIfq65z7FPw2bbiGCy/view

Text Books:

1. Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 2008.
2. Kiat -Seng Yeo, Kaushik Roy, "Low Voltage Low Power VLSI Subsystems", Tata McGraw Hill Publications, 2009.ABCD

Reference Books:

1. Jan M. Rabaey, Massoud Pedram, "Low Power Design Methodologies", Kluwer Academic Publishers, 2010.
2. 2. Prof.Ajit Pal, IIT Kharagpur, NPTEL Lecture series on "Low Power Circuits and Systems", June 2012.
3. 3. P. Chandrakasan, R.W. Broadersen, "Low Power Digital CMOS Design", Kluwer Academic Publishers, 1995.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Apply low-power design concepts to classify power dissipation mechanisms in CMOS integrated circuits. (POs – 1, 3, 4, 5)
2. Classify various power optimization techniques at the circuit and logic level. (POs –1, 3 4, 5)
3. Design low-power low voltage adders and special circuits. (POs – 1, 3, 4, 5)
4. Design low-power low voltage memory circuits using the current generation design style. (POs –1, 3, 4, 5)
5. Analyse different low-power architectures and logic synthesis techniques (POs –1, 3, 4, 5)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester-End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5