RAMAIAH
Institute of Technology

CURRICULUM

Academic year 2026 – 2027

V & VI Semester

B. E. **ELECTRONICS AND COMMUNICATION ENGINEERING**

Batch – 2024

RAMAIAH INSTITUTE OF TECHNOLOGY
(Autonomous Institute, Affiliated to VTU)
(Approved by AICTE, New Delhi & Govt. of Karnataka)
Accredited by NBA & NAAC with A^+ Grade

About the Institute:

In 1962, Dr. M. S. Ramaiah, a visionary philanthropist, established the Gokula Education Foundation with a noble mission to uplift society through education. The same year marked a pivotal moment in technical education in India with the founding of the M S Ramaiah Institute of Technology (MSRIT).

MSRIT offers an impressive array of 18 undergraduate and 15 postgraduate programs, all approved by the All India Council for Technical Education (AICTE). The National Board of Accreditation (NBA) has accredited all eligible programs at the undergraduate (UG) and postgraduate (PG) levels. In March 2021, MSRIT earned an 'A^+' grade from the National Assessment and Accreditation Council (NAAC), underscoring its unwavering commitment to academic excellence. Since 2007, the institute has proudly held Autonomous Status for its UG and PG programs, a prestigious recognition granted by the University Grants Commission (UGC) and Visvesvaraya Technological University (VTU). According to the Ministry of Education, Government of India's NIRF Ranking Framework, MSRIT ranks 75th among 1,584 leading engineering institutions and 31st among 131 architecture schools in India for 2025, highlighting its remarkable impact and leadership in education.

The institute participated in the Technical Education Quality Improvement Program (TEQIP), an initiative of the Government of India. To foster a research culture, the institute has established several specialized centres, including the Centre for Imaging Technologies, the Centre for Advanced Materials Technology, the Centre for Antennas and Radio Frequency Systems (CARFS), the Centre for Cyber Physical Systems, the Schneider Centre of Excellence, the Centre for Bio and Energy Materials Innovation, JSW Centre of Excellence in Power Systems and more. MSRIT boasts a faculty of 380 highly qualified members, 70% of whom hold doctoral degrees, and over 300 scholars currently pursuing Ph.D. degrees.

The Entrepreneurship Development Cell (EDC) and "Ramaiah Evolute" have been established on campus to support startup incubation. MSRIT features a dedicated Placement and Training department, a strong mentoring and proctorial system, a fully equipped sports department, and a spacious, air-conditioned library with a wide range of books and subscriptions to both international and national journals. The Digital Library provides access to online e-journals from renowned publishers, including Elsevier ScienceDirect, IEEE, Taylor & Francis, and SpringerLink. Additionally, the Institute is a member of DELNET, CMTI, and the VTU E- Library Consortium.

The institute features a state-of-the-art auditorium, a well-equipped recording studio, and multiple advanced conference halls with videoconferencing capabilities. Additionally, MSRIT provides excellent hostel accommodations for both boys and girls, ensuring a comfortable living environment. MSRIT alumni have achieved remarkable success, holding prominent positions in India and internationally. They maintain strong connections with the institute through an engaged and active Alumni Association.

Founded on Dr. Ramaiah's unwavering commitment to knowledge and innovation, this remarkable institution continues to inspire generations of students and shape the future of engineering and technology in the country.

About the Department:

The Department of Electronics and Communication was started in 1975 and has grown over the years in terms of stature and infrastructure. The department has well equipped simulation and electronic laboratories and is recognized as a Research Center under VTU. The department currently offers a B. E. program with an intake of 138, and two M. Tech programs, one in Digital Electronics and Communication, and one in VLSI Design and Embedded Systems, with intakes of 30 and 18 respectively. The department has a Center of Excellence in Food Technologies sponsored by VGST, Government of Karnataka. The department is equipped with numerous UG and PG labs, along with R & D facilities. Past and current research sponsoring agencies include DRDO, DST, VTU, ISRO, VGST and AICTE with funding amount worth Rs. 1 crore. The department has modern research ambitions to develop innovative solutions and products and to pursue various research activities focused towards national development in various advanced fields such as Signal Processing, Embedded Systems, Cognitive Sensors and RF Technology, Software Development and Mobile Technology.

VISION OF THE INSTITUTE

To be an Institution of International Eminence, renowned for imparting quality technical education, cutting edge research and innovation to meet global socio-economic needs

MISSION OF THE INSTITUTE

RIT shall meet the global socio-economic needs through

1. Imparting quality technical education by nurturing a conducive learning environment through continuous improvement and customization
2. Establishing research clusters in emerging areas in collaboration with globally reputed organizations
3. Establishing innovative skills development, techno-entrepreneurial activities and consultancy for socio-economic needs

QUALITY POLICY

We at M. S. Ramaiah Institute of Technology strive to deliver comprehensive, continually enhanced, global quality technical and management education through an established Quality Management System complemented by the synergistic interaction of the stake holders concerned

VISION OF THE DEPARTMENT

To evolve into a department of national and international repute for excellence in education and cutting-edge research in the domain of Electronics and Communication Engineering

MISSION OF THE DEPARTMENT

The department will continuously strive to

1. Provide a world-class learning environment that caters to local and global technological and social requirements
2. Initiate research collaborations with academia and industries to perform cutting edge research leading to socio-technological innovations
3. Develop skills for pursuing innovation and entrepreneurial ventures for graduating engineers

PROGRAM EDUCATIONAL OBJECTIVES (PEOs):

PEO1: Acquire knowledge and skills to be employed as successful professionals in their chosen careers

PEO2: Emerge as technologists, researchers, and entrepreneurs through lifelong learning

PEO3: Demonstrate social, ethical, and leadership skills

PROGRAM OUTCOMES (POs):

PO1: Engineering Knowledge: Apply knowledge of mathematics, natural science, computing, engineering fundamentals and an engineering specialization to develop to the solution of complex engineering problems.

PO2: Problem Analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions with consideration for sustainable development.

PO3: Design/Development of Solutions: Design creative solutions for complex engineering problems and design/develop systems/components/processes to meet identified needs with consideration for the public health and safety, whole-life cost, net zero carbon, culture, society and environment as required.

PO4: Conduct Investigations of Complex Problems: Conduct investigations of complex engineering problems using research-based knowledge including design of experiments, modelling, analysis & interpretation of data to provide valid conclusions.

PO5: Engineering Tool Usage: Create, select and apply appropriate techniques, resources and modern engineering & IT tools, including prediction and modelling recognizing their limitations to solve complex engineering problems.

PO6: The Engineer and The World: Analyze and evaluate societal and environmental aspects while solving complex engineering problems for its impact on sustainability with reference to economy, health, safety, legal framework, culture and environment.

PO7: Ethics: Apply ethical principles and commit to professional ethics, human values, diversity and inclusion; adhere to national & international laws.

PO8: Individual and Collaborative Team work: Function effectively as an individual, and as a member or leader in diverse/multi-disciplinary teams.

PO9: Communication: Communicate effectively and inclusively within the engineering community and society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations considering cultural, language, and learning differences.

PO10: Project Management and Finance: Apply knowledge and understanding of engineering management principles and economic decision-making and apply these to one's own work, as a member and leader in a team, and to manage projects and in multidisciplinary environments.

PO11: Life-Long Learning: Recognize the need for, and have the preparation and ability for i) independent and life-long learning ii) adaptability to new and emerging technologies and iii) critical thinking in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSOs):

PSO1: Circuit Design Concepts: Apply basic and advanced electronics for implementing and evaluating various circuit configurations.

PSO2: VLSI and Embedded Domain: Demonstrate technical competency in the design and analysis of components in VLSI and embedded domains.

PSO3: Communication Theory and Practice: Possess application level knowledge in theoretical and practical aspects required for the realization of complex communication systems

Semester wise Credit Breakdown for B.E Degree Curriculum Batch 2024-28

Course Category \ Semester	First	Second	Third	Fourth	Fifth	Sixth	Seventh	Eighth	Total Credits
Basic Sciences (BSC)	08	08	03	03	--	--	--	--	22
Engineering Sciences (ESC)	08	09	--	--	--	--	--	--	17
Humanities, Social Sciences and Management (HSMC)	02	02	--	--	03	03	--	--	10
Ability Enhancement Course (AEC)	02	01	01	01	01	--	--	--	06
Universal Human Values (UHV)	--	--	02	--	--	--	--	--	02
Professional Core Courses (PCC)	--	--	11	12	12	06	04	--	45
Integrated Professional Core Course (IPCC)	--	--	04	04	03		04	--	15
Professional Elective Courses (PEC)	--	--	--	--	03	06	03	--	12
Institutional Open Elective Courses (IOE)	--	--	--	--	--	03	03	--	06
Internship (INT)	--	--	--	--	--	--	--	05	05
Mini Project / Project Work (PW)/Skill Enhancement Course (SDC)	--	--	--	--	--	05	02	13	20
Non Credit Mandatory Courses (NCMC)	--	--	✔	✔	✔	✔	--	--	--
Total Credits	20	20	21	20	22	23	16	18	160

SCHEME OF TEACHING V SEMESTER

SI. No.	Course Code	Course Title	Teaching Department	Category	Credits				Total Contact Hours/Week			
					L	T	P	Total	L	T	P	S
1.	EC51	Communication System-II	ECE	PCC	4	0	0	4	4	0	0	4
2.	EC52	Computer Communication Network	ECE	IPCC	2	0	1	3	2	0	2	2
3.	EC53	CMOS VLSI Design	ECE	PCC	2	1	0	3	2	2	0	2
4.	EC54	Microwave Devices & antennas	ECE	PCC	2	1	0	3	2	2	0	2
5.	ECE55x	Program Elective Course- 1	ECE	PEC	3	0	0	3	3	0	0	3
6.	ECL56	CMOS VLSI Design Lab	ECE	PCC	0	0	1	1	0	0	2	0
7.	ECL57	Microwaves & Antenna Laboratory	ECE	PCC	0	0	1	1	0	0	2	0
8.	AL58	Research Methodology & Intellectual Property Rights	ECE	HSMC	3	0	0	3	3	0	0	3
9.	ECAEC591	Ability Enhancement Course-V	ECE	AEC	1	0	0	1	1	0	0	1
				Total	**17**	**2**	**3**	**22**	**17**	**4**	**6**	**17**
10.	HS510	Environmental Studies*		NCMC	0	0	0	0	-			

*** Environmental Studies is under the category of NCMC, 1-hour teaching per week has to be allocated in the time table.**

NOTE: Minimum of 1 subject should have a Tutorial component of 1 Credit.

Nomenclature: IPCC: Integrated Professional Core Course**, PCC:** Professional Core Course**, HSMC:** Humanity and Social Science & Management Courses**, PEC:** Professional Elective Courses**, AEC–**Ability Enhancement Courses, **NCMC**: Non-credit Mandatory Course
L –Lecture, T – Tutorial, P- Practical/ Drawing
Note: ECE55x, where x=1,

Integrated Professional Core Course (IPCC): Refers to Professional Theory Core Course Integrated with practical of the same course. Credit for IPCC is 03 and its Teaching–Learning hours (L : T : P) can be considered as (2 : 0 : 1). The theory part of the IPCC shall be evaluated both by CIE and SEE. The practical part shall be evaluated only by CIE **(no SEE).** However, questions from the practical part of IPCC can be included in the SEE question paper.
Professional Elective Courses: A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in Engineering and Technology curriculum. Multidisciplinary courses that are added to supplement the latest trend and advanced technology in the selected stream of engineering. Each group provides an option to select one course out of five courses. The minimum student's strength for offering professional electives is 10.

AICTE Activity Points to be earned by students admitted to BE program (For more details refer to Chapter 6, AICTE, Activity Point Program, Model Internship Guidelines):

Every regular student, who is admitted to the 4-year degree program, is required to earn 100 activity points in addition to the total credits earned for the program. Students entering 4 years degree program through lateral entry are required to earn 75 activity points in addition to the total credits earned for the program. The activity points earned by the student shall be reflected on the students VIII semester grade card. The activities to earn the points can be spread over the duration of the course. However, minimum prescribed duration should be fulfilled. Activity points (non-credit) have no effect on SGPA/CGPA and shall not be considered for vertical progression. Incase student fail to earn the prescribed activity points; VIII semester grade card shall be issued only after earning the required activity Points. Students shall be eligible for the award of degree only after the release of the VIII semester grade card.

SCHEME OF TEACHING VI SEMESTER

SI. No.	Course Code	Course Title	Category	Credits				Contact Hours/Week			
				L	T	P	Total	L	T	P	S
1.	AL61	Management & Entrepreneurship	HSMC	3	0	0	3	3	0	0	3
2.	EC62	Embedded System Design	PCC	3	1	0	4	3	2	0	3
3.	ECE63x	Program Elective Course – 2	PEC	3	0	0	3	3	0	0	3
4.	ECE64x	Program Elective Course – 3	PEC	3	0	0	3	3	0	0	3
5.	ECL65	Communication Systems Lab-II	PCC	0	0	1	1	0	0	2	0
6.	ECL66	Embedded System Design Lab	PCC	0	0	1	1	0	0	2	0
7.	ECOE0x	Institutional Open Elective – 1	IOE	3	0	0	3	3	0	0	3
8.	ECP67	Mini Project	PW	0	0	4	4	0	0	0	0
9.	EC68	Technical Skill Enhancement Course	AEC	0	1	0	1	0	2	2	0
			Total	**14**	**2**	**6**	**23**	**-**			
10	PE83	Physical Education	NCMC								
11	YO83	Yoga									
12	NS83	NSS									

NOTE: Minimum of 1 subject should have a Tutorial component of 1 Credit.

LIST OF DEPARTMENT ELECTIVES

SI. No.	Course Code	Course Title	Credits				Contact Hours
			L	T	P	Total	
V Sem (ELECTIVE –I)							
1	ECE551	Advanced Digital Logic Verification	3	0	0	3	3
2	ECE552	Mathematics for M L	3	0	0	3	3

3	ECE553	Operating Systems	3	0	0	3	3

VI Sem (ELECTIVE –II)							
5	ECE631	Digital VLSI Testing	3	0	0	3	3
6	ECE632	Information Theory and Coding	3	0	0	3	3
7	ECE633	Image and Video Processing	3	0	0	3	3
8	ECE634	Robotics	3	0	0	3	3
VI Sem (ELECTIVE –III)							
9	ECE641	Mixed Signal IC Design	3	0	0	3	3
10	ECE642	Computer Architecture	3	0	0	3	3
11	ECE643	Cryptography and Network Security	3	0	0	3	3
12	ECE644	ML and Deep Learning	3	0	0	3	3
VII Sem (ELECTIVE –III)							
14	ECE731	Low Power VLSI Design	3	0	0	3	3
15	ECE732	Multimedia Communication	3	0	0	3	3
16	ECE733	Embedded Linux	3	0	0	3	3
17	ECE734	Computer Vision	3	0	0	3	3
18	ECE735	Nanoelectronics	3	0	0	3	3

Nomenclature, PCC: Professional Core Course**, PEC:** Professional Elective Courses, **IOE:** Institutional Open Elective, **PW:** Mini Project, **INT –** Internship

L –Lecture, T – Tutorial, P- Practical/ Drawing

Note: ECE63x , where x=1,2,3,4
ECE64x , where x=1,2,3,4
ECE73x , where x=1,2,3,4,5
ECOE0x*, where x=1,2,3,4,5.. continued from previous

L –Lecture, T – Tutorial, P- Practical/ Drawing/ Project work

Professional Elective Courses: A professional elective (PEC) course is intended to enhance the depth and breadth of educational experience in Engineering and Technology curriculum. Multidisciplinary courses that are added to supplement the latest trend and advanced technology in the selected

stream of engineering. Each group provides an option to select one course out of five courses. The minimum student's strength for offering professional electives is 10.

Institutional Open Elective Courses:

Students belonging to a particular stream of Engineering and Technology are not entitled for the open electives offered by their parent department. However, they can take an elective offered by other departments, provided they satisfy the prerequisite condition, if any. Registration to open electives shall be documented under the guidance of the Proctor.

Selection of an open elective shall not be allowed if,

1. The candidate has studied the same course during the previous semesters of the program.
2. The syllabus content of open electives is similar to that of the Departmental core courses or professional electives.
3. A similar course, under any category, is prescribed in the higher semesters of the program.
4. The minimum students strength for offering open electives is 10.

Mini-project work: Mini Project is a laboratory-oriented course which will provide a platform to students to enhance their practical knowledge and skills by the development of small systems/applications. Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary Mini- project can be assigned to a group having **not more than 4 students.** The CIE marks shall be awarded by a committee constituted by of the Head of the concerned department. The CIE marks awarded for the Mini-project work shall be based on the evaluation of project report, project presentation skill, and question and answer session as per the rubrics defined by the department. SEE will be conducted by the two examiners appointed by the Institute. SEE marks awarded for the mini project shall be based on the evaluation of project work report, project presentation skill and question and answer session.

AICTE Activity Points to be earned by students admitted to BE program (For more details refer to Chapter 6, AICTE, Activity Point Program, Model Internship Guidelines):

Every regular student, who is admitted to the 4-year degree program, is required to earn 100 activity points in addition to the total credits earned for the program. Students entering 4 years degree program through lateral entry are required to earn 75 activity points in addition to the total credits earned for the program. The activity points earned by the student shall be reflected on the students VIII semester grade card. The activities to earn the points can be spread over the duration of the course. However, minimum prescribed duration should be fulfilled. Activity points (non-credit) have no effect on SGPA/CGPA and shall not be considered for vertical progression. Incase student fail to earn the prescribed activity points; VIII semester grade card shall be issued only after earning the required activity Points. Students shall be eligible for the award of degree only after the release of the VIII semester grade card.

COMMUNICATION SYSTEMS - II	
Course Code: EC51	**Credits: 4:0:0**
Prerequisite: Communication Systems-I	**Contact Hours: 56**
Course Coordinator: C G Raghavendra	

Course Contents

Unit I

Information Theory: Uncertainty, Information, and Entropy. Properties of entropy. Source coding theorem. Discrete memoryless channels. Mutual information. Channel capacity theorem.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117101053

Unit II

Base Band Shaping for Data Transmission: Inter Symbol Interference – Introduction, Nyquist criterion for distortion less base-band binary transmission. Correlative coding, Duo binary coding, Eye pattern

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117101051

Unit III

Detection: Model of digital communication system, Gram – Schmidt orthogonalization, geometric interpretation of signals, Maximum likelihood detection
Correlation receiver, Matched Filter Receiver, Properties of Matched Filter

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117101051

Unit IV

Digital Modulation and Demodulation Techniques: Binary modulation techniques, BPSK, FSK, ASK, QPSK and DPSK systems with signal space diagram, generation, demodulation and error probability.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117101051

Unit V

Spread spectrum modulation: Pseudo noise sequences, Notion of spread spectrum, direct sequence spread coherent BPSK, Signal space dimensionality and processing gain, Frequency Hop spread spectrum and applications of spread spectrum modulation.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://archive.nptel.ac.in/noc/courses/noc20/SEM1/noc20-ee34/

Text Books:

1. Simon Haykin, "Digital Communications", Wiley India Pvt. Ltd., 2006.

Reference Books:

1. Bernard Sklar, "Digital Communications", 2nd Edition, Pearson Education, 2007.
2. Simon Haykin, Michael Moher, "Introduction to Analog and Digital Communication", 2nd Edition, Wiley India Pvt. Ltd., 2012.
3. B. P. Lathi and Zhi Ding, "Modern Digital and Analog Communication Systems", 4th International Edition, Oxford University Press, 2015.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Discuss the different source encoding techniques in the concept of information theory. (POs – 1, 2, 3, 4, 11, PSO – 3)
2. Analyze the performance of the different waveform coding techniques (POs – 1, 2, 3, 4, 11, PSO – 3)
3. Interpret the signal space concepts and maximum likelihood detection. (POs – 1, 2, 3, 4, 11, PSO – 3)
4. Discuss the generation and detection of different digital modulation techniques (POs – 1, 2, 3, 4, 11, PSO – 3)
5. Appreciate the spread spectrum techniques in the digital communication systems. (POs – 1, 2, 3, 4, 11, PSO – 3)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5

COMPUTER COMMUNICATION NETWORK	
Course Code: EC52	**Credits: 2:0:1**
Prerequisite: Communication Systems I	**Contact Hours: 28+28P**
Course Coordinator: Flory Francis, Mamtha Mohan	

Course Contents

Unit I

Network Models: Introduction, Layered tasks, OSI Model: Layered Architecture, Peer-to-Peer Processes, Layers in OSI model, TCP/IP protocol suite, Addressing.

- Pedagogy/Course delivery tools: Chalk, power point presentations and talk.
- Links: https://nptel.ac.in/courses/106105080

Unit II

Data Link Control: Framing, Flow and error control, Noisy Channels: Stop-and-Wait Automatic Repeat Request, Go-Back-N Automatic Repeat Request, Selective Repeat Automatic Repeat Request, HDLC.

- Pedagogy/Course delivery tools: Chalk, power point presentations and talk.
- Links: https://nptel.ac.in/courses/106105080

Unit III

Multiple Accesses: Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA.

Controlled Access: Reservation, Polling, Token Passing, Logical ring and physical topology

- Pedagogy/Course delivery tools: Chalk, power point presentations and talk.
- Links: https://nptel.ac.in/courses/106105080

Unit IV

Network Layer Logical addressing: IPv4 addresses: Classful Addressing, Classless Addressing IPv6 Addresses,

Internet Protocol: Internetworking: Need for Network Layer, Internet as a Connectionless Network, IPv4 datagram format. Transition from Ipv4 to Ipv6.

- Pedagogy/Course delivery tools: Chalk, power point presentations and talk.
- Links: https://nptel.ac.in/courses/106105080

Unit V

Network Layer: Delivery, Forwarding, and Routing Deliver, Unicast Routing Protocols.

Transport layer: Process-to-Process Delivery, TCP, TCP Connection.UDP format and operation

Application Layer: Introduction Namespace, DNS, DNS in the Internet Graphs.

- Pedagogy/Course delivery tools: Chalk, power point presentations and talk.
- Links: https://nptel.ac.in/courses/106105080

PRACTICAL COMPONENT OF IPCC

Using suitable software programming tool, demonstrate the operation of the following programs:

Sl. No.	Experiments: Implement the following in C/C++
1.	For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify the program for the cases i) Without error ii) With error.
2.	Write a program for a HDLC frame to perform Bit stuffing and destuffing a bit in a single frame Character stuffing.
3.	Write a program for a HDLC frame to perform Bit stuffing and destuffing a bit in a single frame
4.	Write a program for distance vector algorithm to find suitable path for transmission
5.	Write a program for encryption and decryption of the text
6.	Implementation of Stop and Wait Protocol and Sliding Window Protocol
Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/ QualNet/ Packet Tracer or any other equivalent tool	
7.	Implement a point to point network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.
8.	Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.
9.	Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.
10.	Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes and obtain congestion windows for different sources/ destinations.

Text Books:

1. Data Communication Networking, Behrouz A Forouzan, 6th Edition, TMH 2022

Reference Books:

1. Computer Networks, James F.Cruz, Keith.W.Ross, Pearson education, 2nd Edition 2003.
2. Introduction to Data communication and networking, Wayne Tomasi, Pearson Education 2007.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Discriminate the functionality between the Layers in OSI model and TCP/IP suite. (PO – 1, 2, PSO - 3)
2. Design protocols used in noiseless channels. (PO – 1, 2, 3, PSO - 3)
3. Distinguish the concepts of multiple access techniques and Controlled Access. (PO – 1, 2, PSO - 3)
4. Configure the logical IPv4 addresses in a network and a subnet. (PO – 1, 2, 3, PSO - 3)
5. Understand the routing algorithms used for networking, TCP and DNS. (PO – 1, 2, PSO - 3)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course out comes addressed**
Internal test-I	30	CO1 & CO2
Internal test-II	30	CO3, CO4 & CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1 & CO2
Lab test	10	CO3, CO4 & CO5
Semester End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5

CMOS VLSI DESIGN	
Course Code: EC53	**Credits: 2:1:0**
Prerequisite: Digital Design	**Contact Hours: 28+28T**
Course Coordinator: Raghuram S	

Course Contents

Unit I

Introduction, CMOS Logic Circuits: VLSI Design Flow, CMOS Transistor Structure, CMOS Inverter, NAND/NOR Gates, Compound gates, Pass-transistor circuits, Sequential Circuits

Layout Design: Layout Design Rules, Layout Design, Stick Diagrams

- Pedagogy/Course delivery tools: Chalk and talk PPT
- www.ee.iitm.ac.in/vlsi/courses/ee5311_2020
  www.cmosvlsi.com

Unit II

CMOS Transistor Theory: C-V Characteristics, V-I Characteristics, MOS Capacitance Models, Non-Ideal V-I Effects, DC Transfer Characteristics, Noise margins, Pass Transistor DC Characteristics

Fabrication: CMOS Processing Technology

- Pedagogy/Course delivery tools: Chalk and talk PPT
- www.ee.iitm.ac.in/vlsi/courses/ee5311_2020
  www.cmosvlsi.com

Unit III

Delay: Timing Definitions, RC Delay Model, Elmore Delay Model, Linear Delay Model, Method of Logical Effort, Buffer Design

Power: Dynamic Power Dissipation, Static Power Dissipation

- Pedagogy/Course delivery tools: Chalk and talk PPT
- www.ee.iitm.ac.in/vlsi/courses/ee5311_2020
  www.cmosvlsi.com

Unit IV

Combinational Circuit Design: Static CMOS, Ratioed Logic, Dynamic CMOS.

Sequential Circuit Design: Sequencing static circuits, setup time, hold time

- Pedagogy/Course delivery tools: Chalk and talk PPT
- www.ee.iitm.ac.in/vlsi/courses/ee5311_2020
  www.cmosvlsi.com

Unit V

Adder Design: Mirror Adder, Carry Propagate Adders: RCA Design, Carry Skip, Carry Look ahead, Carry Select Adders, Tree Adders: Brent-Kung, Kogge-Stone, Sklansky Adders

Multipliers: Array Multiplication, Booth Encoding

- Pedagogy/Course delivery tools: Chalk and talk PPT
- www.ee.iitm.ac.in/vlsi/courses/ee5311_2020
  www.cmosvlsi.com

Text Books:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuit and Systems Perspective", 4th Edition, Pearson Education, 2015.

Reference Books:

1. Jan Rabaey, B. Nikolic, A. Chandrakasan, "Digital Integrated Circuits: A Design Perspective", 2nd Edition, Pearson, 2003.
2. Morris Mano, Michael Ciletti, "Digital Design", 5th Edition, Pearson Education, 2013.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Design digital circuits and layouts for CMOS technology. (POs – 1, 2, 3, 4, 5, 7, 8, 9, 10, 11 PSO – 2)
2. Predict the current flowing through a CMOS transistor, and the power consumed during the operation of such circuits (POs – 1, 2, 3, 4, 5, 7, 8, 9, 10, 11 PSO – 2)
3. Evaluate the power consumption and delay in MOS logic circuits, and thereby design a circuit to satisfy constraints (POs – 1, 2, 3, 4, 5, 7, 8, 9, 10, 11 PSO – 2)
4. Analyze the performance of various MOS circuit families and the associated timing constraints (POs – 1, 2, 3, 4, 5, 7, 8, 9, 10, 11 PSO – 2)
5. Describe various connection configurations to realize datapath elements and analyze their operating speed (POs – 1, 2, 3, 4, 5, 7, 8, 9, 10, 11 PSO – 2)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Mini-Project	20	CO1, CO2, CO3, CO4, CO5
Semester End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5

MICROWAVE DEVICES AND ANTENNAS	
Course Code: EC54	**Credits: 2:1:0**
Prerequisite: Electro Magnetics	**Contact Hours: 28+28T**
Course Coordinator: Sujatha B	

Course Contents

Unit I

Multiport Microwave Network Analysis: Impedance, admittance and transmission matrices of reciprocal microwave networks, scattering matrix – reciprocal and lossless networks (only statement), Basic properties of dividers and couplers – three-port networks, four-port networks; T-junction power divider – lossless divider, resistive divider, Wilkinson power divider – even-odd mode analysis.

- Pedagogy/Course delivery tools: Chalk and talk
- Links : https://youtu.be/cnvYxtEto7U
  https://youtu.be/tKZ-lAzYLys
  https://youtu.be/7bjeIBiyWyM from NPTEL

Unit II

Microwave Devices and Tubes: PIN diode and applications, RWH theory, Gunn diodes– Gunn Effect, modes of operation. Two cavity klystron amplifiers, Reflex Klystron - Mathematical analysis of power and efficiency, Traveling Wave Tubes, Magnetron Oscillators (only construction and working).

- Pedagogy/Course delivery tools: Chalk and talk
- Links : https://youtu.be/2SxSBMum4gc (IIT Bombay)
  https://youtu.be/366BVdmcUxk (IIT Roorke)

Unit III

Fundamentals of Antenna: Principle of antenna, fields from oscillating dipole, antenna field zones, basic antenna parameters, patterns, beam area, Radiation intensity, beam efficiency, directivity and gain, antenna aperture, effective height and radio communication link (Friis formula).

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://youtu.be/wx_tIvaajAI (NPTEL)
  https://youtu.be/h51mFbIgZRI (IIT karagpur)

Unit IV

Point source and Arrays: Point source, Types of Arrays (Broad side, End fire, Extended End fire), Arrays of two point sources, linear array of n-isotropic point sources of equal amplitude and spacing, pattern multiplication.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://youtu.be/2q9cJmNduvc (IIT Bombay)
  https://youtu.be/4gsq-UgCarc (IIT Karagpur)

Unit V

Thin Linear Antennas: Introduction, radiation resistance of short electric dipole, thin linear antenna, field components of λ/2 (hertz) dipole antenna, radiation resistance of λ/2 antenna, Yagi-Uda antenna **Aperture and Printed Antennas**: Rectangular Pyramidal Horn antenna analysis and design, Micro strip rectangular patch antenna design.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://youtu.be/aiGoqd-0XSk (IIT Karagpur) https://youtu.be/Y1RBxyk9Cow (IIT Bombay)

Text Books:

1. David M. Pozar, "Microwave Engineering", 4th Edition, Wiley publication , 2013.
2. Samuel Y Liao, "Microwave Devices and Circuits", 3rd Edition, Pearson Education, 2021.
3. John D Kraus, Ronald J Marhetka, Ahmad S Khan, "Antennas and Wave Propagation", 5th Edition, Tata McGraw Hill, 2017.

Reference Books:

1. Annapurna Das and Sisir K Das, "Microwave Engineering", 3rd Edition, McGraw-Hill, 2015.
2. Constantine A Balanis, "Antenna, Theory, Analysis & Design", 4th Edition, John Wiley & Sons, 2016.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Apply the properties of scattering parameters to obtain the S-matrix of microwave components and circuits. (POs – 1, 2, 3, 7, 9, 11, PSOs –1, 3)
2. Illustrate the significance of various microwave passive devices and tubes. (POs – 1, 2, 3, 7, 9, 11, PSOs –1, 3)
3. Describe the parameters of antennas. (POs – 1, 2, 3, 7, 9, 11, PSOs –1, 3)
4. Design different types of arrays and study the concept of pattern multiplication. (POs – 1, 2, 3, 7, 9, 11, PSOs –1, 3)
5. Explore the field components and radiation resistance of various antennas. (POs – 1, 2, 3, 7, 9, 11, PSOs –1, 3)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5

RESEARCH METHODOLOGY AND INTELLECTUAL PROPERTY RIGHTS	
Course Code: AL58	**Credits: 3:0:0**
Prerequisite: Nil	**Contact Hours: 42L**
Course Coordinator: -	

Course Contents

Unit I

Research Methodology Introduction: Meaning of Research, Objectives of Research, Types of Research, Ethics in Research, Types of Research Misconduct. Literature Review and Technical Reading, New and Existing Knowledge, Analysis and Synthesis of Prior Art, Bibliographic Databases, Conceptualizing Research, and Critical and Creative Reading. **Citations:** Functions and Attributes, Impact of Title and Keywords on Citations, Knowledge flow through Citations, Acknowledgments, and Attributions.

- Pedagogy/Course delivery tools: Chalkboard, PowerPoint presentations: Chalk and talk
- Link: https://onlinecourses.nptel.ac.in/noc22_ge08/preview

Unit II

Research Design: Need for Research Design, Important Concepts Related to Research Design: Dependent and Independent Variables, Extraneous Variable, Variable, Common Control, Confounded Relationship, Research Hypothesis, Experimental and Control Groups, Treatments.

Experimental Designs: Introduction to Randomized Block Design, Complete Randomized Design, Latin Square Design, and Factorial Design.

- Pedagogy/Course delivery tools: Chalkboard, PowerPoint presentations: Chalk and talk
- Link: https://onlinecourses.nptel.ac.in/noc22_ge08/preview

Unit III

Method of Data Collection: Primary and Secondary Data Collection. **Sampling Design:** Sampling fundamentals, Measurement, and Scaling Techniques, Criteria of Selecting a Sampling Procedure, Characteristics of a Good Sample Design, and Types of Sample Design. **Data Analysis:** Testing of Hypotheses: Null Hypothesis, Alternative Hypothesis, Type I and Type II Errors, Level of Significance. Procedure for Hypothesis Testing: Mean, Variance, Proportions. Chi-square Test, Analysis of Variance (One Way ANOVA), and Covariance (ANOCOVA)

- Pedagogy/Course delivery tools: Chalkboard, PowerPoint presentations: Chalk and talk
- Link: https://onlinecourses.nptel.ac.in/noc23_ge36/preview

Unit IV

Introduction to IPR: Different forms of IPR, Role of IPR in Research and Development. TRIPS Agreement, Patent Cooperation Treaty (PCT).

Patents: Brief history of Patents-Indian and Global Scenario, Principles Underlying Patent Law, Types of Patent Applications in India, Procedure for Obtaining a Patent. Non Patentable Inventions. Rights Conferred to a Patentee, Basmati Rice Patent Case.

- Pedagogy/Course delivery tools: Chalkboard, PowerPoint presentations: Chalk and talk
- Link: https://archive.nptel.ac.in/courses/110/105/110105139/

Unit V

Design: What is a Design? Essential Requirements for a Registrable Design, Procedure of Registration of a Design, **Trademarks:** Essentials of a Trademark, Registration, and Protection of Trademarks, Rights Conferred by Registration of Trademarks, Infringements, Types of Reliefs, Case Studies. **Copyrights:** Characteristics of Copyrights, Rights Conferred by Registration of Copyrights, Registration of Copyrights, Infringements, Remedies against Infringement of Copyrights, Case studies

- Pedagogy/Course delivery tools: Chalkboard, PowerPoint presentations: Chalk and talk
- Link: https://archive.nptel.ac.in/courses/110/105/110105139/

Text Books:

1. C. R Kothari, Gourav Garg, Research Methodology – Methods and Techniques. New Age International Publishers.
2. Dr. B L Wadehra – Law relating to Intellectual property. Universal Law Publishing Co.
3. Dipankar Deb, Rajeeb Dey, Valentina E. Balas "Engineering Research Methodology", ISSN 1868-4394 ISSN 1868-4408 (electronic), Intelligent Systems Reference Library, ISBN 978-981-13-2946-3 ISBN 978-981-13-2947-0 (eBook), https://doi.org/10.1007/978-981-13-2947-0.

References Books:

1. David V. Thiel "Research Methods for Engineers" Cambridge University Press, 978-1-107-03488-4

Course Outcomes (COs):

At the end of the course, students' will be able to

1. Possess the knowledge of research and conduct a literature review**.** (PO-7, PO-1, PO-11)
2. Apply the knowledge of research design and design of experiments. (PO-4, PO-7, PO 9, PO-11)
3. Analyse data collection methods, analysis, and sampling design. (PO-4, PO-7, PO-9, PO-11)
4. Understand the global and Indian scenarios of patents and patent applications. (PO-7, PO-9, PO-11)
5. Acquire the requirements of registration and infringements related to trademarks, copyrights, and designs. (PO-7, PO-9, PO-11)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5

ABILITY ENHANCEMENT COURSE – V ADVANCED VERILOG	
Course Code: ECAEC591	**Credits: 1:0:0**
Prerequisite: Digital Design	**Contact Hours: 14L**
Course Coordinator: V Anandi	

Course Content

1. Design a model to implement the minterm list given by using a UDP.
2. Design a 8-bit ALU with basic operations such as addition and subtraction and logical operations such as AND, NOR etc.
3. Sequential circuits Flip flops, Register and counters
4. FSM for a sequence detector (e.g., 111, without overlap)
5. Starting with a basic arbiter, design a Round Robin Arbiter
6. 4x4 asynchronous read and read/write memory
7. 4-bit Array Multiplier with and without Pipelining
8. 16-bit Brent-Kung Adder Design
9. 8-bit Radix-4 Multiplier with Booth Encoding block
10. Design a basic MAC unit and its pipelined implementation.
11. FIR filter with parameterizable taps and coefficients using Verilog
12. FIR filter with pipelining

Text Book:

1. Brock LaMeres J," Quick Start Guide to Verilog", Springer Nature Switzerland AG; 1st ed. 2019 edition

Reference books:

1. Michael D Ciletti, "Advanced Digital Design with the Verilog HDL", 2nd Edition Pearson, 2018
2. Samir Palnitkar, "Verilog HDL- A Guide to Digital Design and Synthesis", 2nd Edition Prentice Hall, 2010

Course Outcomes

1. Design combinational logic circuits and verify the functionality using HDL (POs –1, 2,3, 5, PSO – 1,2)
2. Implement sequential logic circuits and verify using HDL (POs–1, 2, 3, 5, PSO –1, 2)
3. Design and simulate FSM Models (POs – 1, 2, 3, 5, 9, 10,
4. Describe read and write memory operations using HDL (POs – 1, 2, 3, 5, PSO –1, 2)
5. Realize FIR filters and pipelining operations using HDL (POs – 1, 2, 3, 5, PSO –1, 2)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Weekly evaluation of laboratory manuals/records after the conduction of every experiment	30	CO1, CO2, CO3, CO4, CO5
Practical test	20	CO1, CO2, CO3, CO4, CO5
Semester End Examination (SEE)	50	CO1, CO2, CO3, CO4, CO5

CMOS VLSI DESIGN LAB	
Course Code: ECL 56	**Credits: 0:0:1**
Prerequisite: Digital Design	**Contact Hours: 28P**
Course Coordinator: Raghuram S	

Course Content

List of Experiments

1. Front End ASIC Design Flow – Combinational Circuits
2. Front End ASIC Design Flow – Sequential Circuits
3. Calculation of propagation delay
4. Design of Basic CMOS Gates, Functionality Verification
5. V-I Characteristics of MOS Transistors
6. CMOS Inverter Transient and DC Analysis
7. Calculation of FO4 delay
8. Inverter chain design
9. Dynamic CMOS Circuits
10. Hold Time Measurement
11. Carry Lookahead Adder – RTL Design and Synthesis
12. Inverter – layout: DRC, LVS

- Pedagogy/Course delivery tools:
- Virtual Lab: https://vlsi-iitg.vlabs.ac.in/ http://vlabs.iitkgp.ac.in/mvlsi/

Text Books:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuit and Systems Perspective", 4th Edition, Pearson Education, 2015.

Reference Books:

1. Jan Rabaey, B. Nikolic, A. Chandrakasan, "Digital Integrated Circuits: A Design Perspective", 2nd Edition, Pearson Education, 2003.
2. Morris Mano, Michael Ciletti, "Digital Design", 5th Edition, Pearson Education, 2013.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Employ the digital design tools for HDL design entry, simulation, and synthesis (POs – 2, 3, 4, 5, 7, 8, 9,11, PSO – 2)
2. Create and verify functionality of various gates at the transistor level (POs – 2, 3, 4, 5, 7, 8, 9,11, PSO – 2)
3. Measure circuit performance parameters by performing simulations of circuit configurations (POs – 2, 3, 4, 5, 7, 8, 9,11, PSO – 2)
4. Use tools to characterize processes by conducting suitable experiments (POs – 2, 3, 4, 5, 7, 8, 9,11, PSO – 2)

5. Create the layout for simple gates, and perform DRC and LVS Checks (POs – 2, 3, 4, 5, 7, 8, 9,11, PSO – 2)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Weekly evaluation of laboratory manuals/records after the conduction of every experiment	30	CO1, CO2, CO3, CO4, CO5
Practical test	20	CO1, CO2, CO3, CO4, CO5
Semester End Examination (SEE)	50	CO1, CO2, CO3, CO4, CO5

MICROWAVES AND ANTENNA LABORATORY	
Course Code: ECL57	**Credits: 0:0:1**
Prerequisite: Microwaves and Antennas	**Contact Hours: 28P**
Course Coordinator: Sujatha B	

Course Content

List of Experiments:

1. Determination of the modes, transit time, electronic timing range, and sensitivity of the Klystron source.
2. Measurement of VSWR, Guide Wavelength, Operating frequency, and Impedance of unknown load (Horn antenna)
3. Determination of V-I characteristics of GUNN diode, and measurement of guide Wavelength, Frequency and VSWR applying Gunn source.
4. Determination of coupling coefficient and insertion loss of Branch line and Backward directional couplers (Microstrip components).
5. Determination of coupling coefficient and power division of a hybrid tee (Magic tee).
6. Measurement of power division and isolation characteristics of a 3-dB power divider.
7. Measurement of resonant frequency and calculate the permittivity of microstrip ring resonator.
8. Measurement of coupling coefficient, isolation and insertion loss of rectangular waveguide directional coupler.
9. Experimental studies on Horn antenna radiation pattern and determine the beam area, directivity and gain of horn antenna.
10. Experimental studies of radiation pattern of Micro strip Yagi-Uda antenna and determine the beam area, directivity and gain of Yagi – Uda antenna.
11. Experimental studies of radiation pattern of Micro Strip Dipole antenna and determine the beam area, directivity and gain of dipole antenna
12. Implementation of radiation pattern of Arrays of *n* isotropic Antenna using 'C'.
13. Design and Simulation of a Dipole Antenna using HFSS

References:

1. David M. Pozar, "Microwave Engineering", 3rd Edition, Wiley, 2011.
2. Samuel Y Liao, "Microwave Devices and Circuits", 3rd Edition, Pearson, 2011.
3. John D. Kraus, Ronald J. Marhefka and Ahmad S Khan "Antennas and Wave Propagation", 4th Edition, McGraw-Hill Publications, 2017.

Course Outcomes (COs):

1. Analyze the characteristics of multiport microwave networks (POs – 1, 2, 5, 6, 7, 8, 9, PSO -3)
2. Interpret the characteristics of microwave oscillators and measure the impedance of the unknown load (POs – 1, 2, 5, 6, 7, 8, 9, PSO -3)
3. Obtain the radiation pattern and calculate the antenna parameters (POs – 1, 2, 5, 6, 7, 8, 9, PSO -3)
4. Measure the resonant frequency of the ring resonator and analyze its permittivity (POs – 1, 2, 5, 6, 7, 8, 9 PSO -3)
5. Analyze V-I characteristics of GUNN diode (POs – 1, 2, 5, 6, 7, 8, 9, PSO -3)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Weekly evaluation of laboratory manuals/records after the conduction of every experiment	30	CO1, CO2, CO3, CO4, CO5
Practical test	20	CO1, CO2, CO3, CO4, CO5
Semester End Examination (SEE)	50	CO1, CO2, CO3, CO4, CO5

V Semester Electives

ADVANCED DIGITAL LOGIC VERIFICATION	
Course Code: ECE551	**Credits: 3:0:0**
Prerequisite: Digital Design	**Contact Hours: 42L**
Course Coordinator: Reshma Verma	

Course Contents

Unit I

Verification Concepts: Concepts of Verification, Importance of verification, Stimulus vs Verification, Test bench generation, Functional verification approaches, Typical verification flow, Stimulus generation, Direct testing, Coverage: Code coverage and Functional coverage, Coverage plan.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: http://www.testbench.in/TS_00_INDEX.html

Unit II

System Verilog – Language Constructs: System Verilog Constructs- Data types: Two state data, Strings, Arrays: Queues, Dynamic and Associative Arrays, Structs, Enumerated types. Program blocks, modules, interfaces, Clocking ports, Mod ports.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: http://www.testbench.in/SV_00_INDEX.html

Unit III

System Verilog – Classes and Randomization: SV classes: Language evolution, Classes and Objects, Class Variables and Methods, Class Instantiation, Inheritance and Encapsulation, Polymorphism, Randomization: Directed vs Random Testing, Randomization, Constraint driven Randomization.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: http://www.testbench.in/CR_00_INDEX.html

Unit IV

System Verilog – Assertions and Coverage: Assertions: Introduction to assertion-based verification, Immediate and concurrent assertions, Coverage driven assertion, Motivation, types of coverage, Cover group, Cover point, Cross coverage, Concepts of binning and event sampling.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://www.chipverify.com/systemverilog/systemverilog-assertions

Unit V

Test bench: Layered test bench architecture, Introduction to Universal verification methodology, Overview of UVM, Base classes and simulation phases in UVM, UVM environment structure, Connecting DUT – Virtual Interface.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://www.chipverify.com/uvm/uvm-introduction

Text Books:

1. Chris Spear, Greogory J Tumbush, ―System Verilog for Verification – A Guide to Learning Test Bench Language Features‖, Springer, 2012.
2. Stuart Sutherland, ―RTL Modeling with System Verilog for Simulation and Synthess: using System Verilog for ASIC and FPGA Design‖, 1st Edition, Create Space Independent Publishing Platform, 2017.

References Books:

1. System Verilog 3.1a LRM, Accellera‘s Extensions to Verilog
2. Sasan Iman, ―Step by Step Functional Verification with System Verilog and OVM ‖, Hansen Brown Publishing, 2008.
3. UVM Cookbook, Mentor Graphics
4. www.asic-world.com
5. www.testbench.in
6. www.chipverify.com/systemverilog/systemverilog-class
7. Seer recordings

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Express the principles of HDL verification. (POs – 1, 2, 3, 4, 5,11, PSO – 2)
2. Apply OOPs concepts in System Verilog verification environment. (POs – 1, 2, 3, 4, 5, 11, PSO – 2)
3. Construct basic verification environment using System Verilog (POs – 1, 2, 3, 4, 5, 11, PSO – 2)
4. Generate random stimulus and track functional coverage using System Verilog (POs – 1, 2, 3, 4, 5, 11, PSO – 2)
5. Appreciate the concepts of layered test bench architecture and its components (POs – 1, 2, 3, 4, 5, 11, PSO – 2)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1 & CO2
Internal test-II	30	CO3, CO4 & CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Project	20	CO1, CO2, CO3, CO4 & CO5
Semester End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5

MATHEMATICS FOR MACHINE LEARNING	
Course Code: ECE552	**Credits: 3:0:0**
Prerequisite: Nil	**Contact Hours: 42L**
Course Coordinator:	

Course Contents

Unit I

Linear Algebra: Systems of linear equations, Matrices, solving systems of linear equations, Vector spaces, Linear independence, Basis and Rank, Change of basis

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://www.digimat.in/nptel/courses/video/111107137/L01.html

Unit II

Matrix Decomposition: Determinant and Trace, Eigen values and Eigen vectors, Cholesky decomposition, Eigen decomposition and diagonalization, Singular Value Decomposition (SVD)

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://digimat.in/nptel/courses/video/111107137/L12.html

Unit III

Analytic Geometry: Norms, Inner product, Lengths and Distances, Angles and Orthogonality, Orthogonal Basis, Orthogonal Projections, Rotations

- Pedagogy/Course delivery tools: Chalk and talk
- https://www.digimat.in/nptel/courses/video/111107137/L07.html
- https://digimat.in/nptel/courses/video/111107137/L27.html

Unit IV

Probability and Distribution: Probability concepts, Conditional probability, Bayes' Theorem, Discrete and Continuous random variables and distributions, Expectation and its interpretations, Standard discrete and continuous distribution functions, Central Limit theorem

- Pedagogy/Course delivery tools: Chalk and talk
- Link:

Unit V

Continuous Optimization: Optimization using Gradient Descent, Constrained optimization and Lagrange multipliers, Convex optimization

- Pedagogy/Course delivery tools: Chalk and talk
- Link: https://digimat.in/nptel/courses/video/111107137/L40.html

Text Books:

1. M. P. Deisenroth, A. A. Faisal, C. S. Ong, "Mathematics for Machine Learning", 1st edition, Cambridge University

References Books:

1. Papoulis, S. Unnikrishna Pillai, "Probability, Random Variables and Stochastic Processes", 4th Edition, McGraw Hill, 2002.
2. David C Lay, "Linear Algebra and its Applications", 4th Edition, Pearson Education, 2018.
3. David J. C. MacKay, "Information Theory, Inference and Learning Algorithms", Cambridge University Press, 2003.
4. Stephen Boyd, Lieven Vandenberghe, "Convex Optimization", Cambridge University Press, 2004

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Solve systems of linear equations using multiple methods and demonstrate understanding of the concepts of vector space (POs – 1, 2, 3, 7, 11, PSO – 3)
2. Compute and interpret eigenvalues and eigenvectors, orthogonality and diagonalization (POs – 1, 2, 3, 5, 7, 11, PSO – 3)
3. Apply principles of matrix algebra and orthogonality to transformations (POs –1, 2, 3, 7, 11, PSO – 3)
4. Appraise basics of probability and distribution (POs – 1, 2, 3, 7, 11, PSO – 3)
5. Formulate optimization problems for given situations and apply different methods of optimization (POs – 1, 2, 3, 5, 7, 11, PSO – 3)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5

OPERATING SYSTEMS	
Course Code: ECE553	**Credits: 3:0:0**
Prerequisite: Nil	**Contact Hours: 42L**
Course Coordinator: Sara Mohan George	

Course Contents

Unit I

Introduction to Operating Systems: Concept, Components of Operating System, Operating System Operations, Computing Environment. Abstract View of OS: User view, System View, System Calls: Concept, Types of System Calls. Distributed Operating systems

Scheduling: Introduction, First In, First Out (FIFO), Shortest Job First (SJF), Shortest Time-to-Completion First (STCF), Round Robin.

Forensics and Operating Systems: Introduction, Forensics, Memory forensics – real memory and addressing, Virtual memory.

- Pedagogy/Course delivery tools: Chalk, Power point presentations and talk
- Links: https://nitdgp.ac.in/ckfinder/uploads/userfiles/files/btech_syllabus_copy2_latest.pdf https://a.impartus.com/ilc/#/course

Unit II

Process

Synchronization: Avoidance and Concurrency: Introduction, Thread creation, Thread completion.

Deadlocks: Deadlocks in resource allocation, Resource state modeling, Deadlock detection algorithm (Avoidance), and Deadlock prevention.

- Pedagogy/Course delivery tools: Chalk, Power point presentations and talk
- Links: https://nitdgp.ac.in/ckfinder/uploads/userfiles

Unit III

Paging and Segmentation: Introduction, Page table, Smaller tables, Hybrid approach: Paging and Segments, Multi-level page tables segmentation, Generalized base/bounds.

File Systems and Directories: File system interface, Making, Reading and deleting directories, File system implementation, Inode, Directory organization, Free space management.

- Pedagogy/Course delivery tools: Chalk, Power point presentations and talk
- Links: http://nitrr.ac.in/downloads/syl_new/CSE/5th%20sem http://nitrr.ac.in/downloads/syl_new/CSE/5th%20sem

Unit IV

Mobile Operating Systems: Android- Filesystem Layout, Malware, Backups IOS- Filesystem Layout, Malware and jail breaking, iCloud backup.

Linux Operating System: Introduction to Linux OS, Basic Commands of Linux OS. Process Management, Memory Management & File Management Commands and System Calls.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: http://bvicam.in https://onlinecourses.swayam2.ac.in/cec22_cs23/preview

Unit V

Tracking Artifacts: Introduction, Location information, Document tracking, shortcuts. Newer Technologies: Introduction, Virtualization, Cloud Computing, Wearables, Drones

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://a.impartus.com/ilc/#/course/96234/452

Text Books:

1. Remzi Arpaci-Dusseau, Andrea Arpaci-Dusseau, "Operating Systems: Three Easy Pieces", 1st Edition, Arpaci-Dusseau Books, 2018.
2. Ric Messier, "Operating Systems Forensics", 1st Edition, Elsevier Inc., 2015.
3. Sumitabha Das, "Unix concept and Programming", McGraw Hill education, 4th Edition, 2015.

References Books:

1. Silberschatz, Galvin, Greg, "Operating System Concepts", Wiley and Sons, 9th Edition, 2015.
2. William Stallings, "Operating Systems: Internals and Design Principles", 9th Edition, Pearson Education, 2018.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Explain the structure and functions of operating systems along with their components, types and working, scheduling algorithms & acquire knowledge of forensics in mobile operating systems. (PO – 1,2,5,11, PSO – 3)
2. Illustrate process synchronization and deadlock avoidance. (POs – 1, 2,5,11, PSO – 3)
3. Elaborate on segmentation and file system organization. (POs – 1, 2,5,11, PSO – 3)
4. Acquire knowledge on mobile operating systems and make use of appropriate Linux commands for memory management, file management and directory management (POs – 1,2,5,11, PSO – 3)
5. Obtain innovative knowledge of newer technologies. (POs – 1, 2,5,11, PSO – 3)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2
Lab	10	CO1, CO2, CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

ENVIRONMENTAL STUDIES	
Course Code: HS510	**Credits: 0:0:0**
Prerequisite: Nil	**Contact Hours: 14L**
Course Coordinator: -	

Course Content

Unit I

Environment, Ecology and Biodiversity Definition, scope, and importance. Multidisciplinary nature of Environmental studies. Food chain and food web. Energy flow and material cycling in the ecosystem. Biodiversity and threats to biodiversity. Concept of sustainable development:Definition, objectives, and applications.

- Pedagogy/Course delivery tools: Chalk and Talk, PowerPoint presentations, Videos, Models
- Link: https://youtu.be/I_bnGkviWOU
  https://youtu.be/Ar04qG1P8Es

Unit II

Natural resources Forest resources: Ecological importance of forests. Water resources: Global water resources distribution. Mineral resources: Environmental effects of extracting and processing Mineral resources. Food resources: Effects of modern agriculture. Land resources: Soil erosion and Desertification.

- Pedagogy/Course delivery tools: Chalk and Talk, PowerPoint presentations, Videos
- Link: https://youtu.be/vsXv3anIBSU
  https://youtu.be/1rOVPqaUyv8

Unit III

Energy sources Growing energy needs. Conventional and non-conventional / Renewable and Non-renewable energy sources. Bio Energy-Ethanol and Bio mass energy. Energy of the future – Hydrogen fuel cells and Nuclear energy. Environmental Impact Assessment (EIA): Definition, Objectives and benefits. Step by step procedure of conducting EIA.

- Pedagogy/Course delivery tools: Chalk and Talk, PowerPoint presentations, Animations, Models
- Link: https://youtu.be/mh51mAUexK4
  https://youtu.be/XS-eXqppf_w

Unit IV

Environmental pollution Definition, Causes, Effects and control measures of Water pollution, Air pollution and Soil/ land pollution. Management of Municipal Solid Waste and treatment methods of municipal solid waste.

- Pedagogy/Course delivery tools: Chalk and Talk, PowerPoint presentations, Videos
- Link: https://youtu.be/NRoFvz8Ugeo
  https://youtu.be/DAQapF-F4Vw

Unit V

Environmental protection Global warming and Climate change, Acid rain, Ozone layer depletion. Salient features of Environmental Protection Act, Air & Water Acts. Functions of Central and State Pollution Control Boards.

- Pedagogy/Course delivery tools: Chalk and Talk, PowerPoint presentations, Videos, Open source softwares
- Link: https://youtu.be/iV-BvYwl4Y8
  https://youtu.be/BYqLRGawoH0

Text Books:

1. Dr. S M Prakash – Environmental Studies, Elite Publishers, 2007.

Reference Books:

1. P. Venugopala Rao – Principles of Environmental Science & Engineering Prentice Hall of India, 1st edition, 2006.

Web links and video Lectures (e- Resources):

1. https://youtu.be/I_bnGkviWOU
2. https://youtu.be/vsXv3anIBSU
3. https://youtu.be/mh51mAUexK4
4. https://youtu.be/NRoFvz8Ugeo
5. https://youtu.be/iV-BvYwl4Y8

Course Outcomes (COs):

At the end of the course, the student will be able to:

1. Describe the importance of environmental studies, sustainable development and biodiversity (PO-1, 7)
2. Explain the importance and conservation of impacts of natural resources (PO-1, 7)
3. Distinguish the energy sources and identify the alternative energy sources for sustainable development (PO-1, 7)
4. Identify the causes, effects and control measures of pollution in developmental activities (PO-1, 7)
5. Outline the current environmental issues and the role of the agencies for environmental protection (PO-1, 7)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment tool	**Marks**	**Course outcomes attained**
Internal Test-I	30	CO1, CO2, CO3
Internal Test-II	30	CO4, CO5
Average of the two internal test shall be taken for 30 marks		
Other components		
Assignment – MCQ, Objectives	10	CO1, CO2
Assignment – Quiz, Group presentation	10	CO3, CO4
Semester End Examination (SEE)	50	CO1, CO2, CO3, CO4, CO5

VI SEMESTER

MANAGEMENT & ENTREPRENEURSHIP	
Subject Code: AL61	**Credits: 3:0:0**
Pre requisites: NIL	**Contact Hours: 42L**
Course Coordinators: Dr. M Shilpa/ Dr. M Rajesh	

Course Content

Unit I

Introduction to Management: Definition of Management, Its nature and purpose, Contributions of F.W. Taylor and Henry Fayol to management theory, Functions of managers. **Planning:** Types of plans, Steps in planning, the planning process, Management by Objectives (MBO) **Organizing:** The nature and purpose of organizing, Formal and informal organization. Organization levels and Span of management, Principle of span of management, the structure and process of organizing

- Pedagogy: Chalk and Talk, PowerPoint Presentations
- Links: https://onlinecourses.nptel.ac.in/noc23_mg33/preview https://www.digimat.in/nptel/courses/video/110107150/L01.html

Unit II

Staffing: Situational factors affecting staffing. **Leading:** Human factors in managing, definition of leadership, Ingredients of leadership **Controlling:** Basic control process, Critical control points and standards, Control as a feedback system, Feed forward control, Requirements for effective controls.

- Pedagogy: Chalk and Talk, PowerPoint Presentations
- Links: https://nptel.ac.in/courses/110107150

Unit III

Introduction to Entrepreneurship: The Foundations of Entrepreneurship: What is an Entrepreneurship? The benefits of Entrepreneurship, The potential drawbacks of Entrepreneurship; Inside the Entrepreneurial Mind: From Ideas to Reality: Creativity, Innovation and Entrepreneurship, Creative Thinking, Barriers to Creativity

- Pedagogy: Chalk and Talk, PowerPoint Presentations
- Links:https://www.youtube.com/watch?v=Hgj_kRrvbhQ&list=PL7oBzLzHZ1wXW3mtolxV5nIGn48NLKwrb

Unit IV

The Entrepreneurial Journey: Crafting a Business Plan: The benefits of creating a business plan, the elements of a business plan; Forms of Business Ownership and Buying an Existing Business: Sole proprietorships and partnership.

Launching the Business: Franchising and the Entrepreneur: Types of Franchising, the benefits of buying a Franchise

- Pedagogy: Chalk and Talk, PowerPoint Presentations
- Links:https://www.youtube.com/watch?v=Tzzfd6168jk&list=PLyqSpQzTE6M8EGZbmNUuUM7Vh2GkdbB1R https://www.youtube.com/watch?v=5RMqxtMwejM&list=PLyqSpQzTE6M9zMKj_PSm81k9U8NjaVJkR

Unit V

Small Scale Industry: Definition, Characteristics, types, role of SSI in Economic Development, steps to start SSI- Govt. Policy towards SSI, Institutional support- TECKSOK, KIADB, KSSIDC, KSIMC, DIC, NSIC, SIDBI, KSFC.

- Pedagogy: Chalk and Talk, PowerPoint Presentations
- Links:https://www.nptel.ac.in/courses/110/105/110105067/

Text Books:

1. Harold Koontz, H. Weihrich, and A.R. Aryasri, Principles of Management, Tata McGraw-Hill, New Delhi, 2004.
2. Essentials of Entrepreneurship and Small Business Management – Norman Scarborough & Jeffrey Cornwall (Pearson, 2016)
3. Management and Entrepreneurship by K. R. Phaneesh, Sudha Publications, Bangalore

References:

1. Innovation & Entrepreneurship – Peter Drucker (Harper, 2006)
2. Entrepreneurship: The Art, Science, and Process for Success – Charles Bamford & Garry Bruton (McGraw-Hill, 2015)
3. Managent and Enterpreneuship-NVR Naidu, T Krishna Rao, I.K. International Publishing House Pvt. Ltd.@ 2008
4. Poornima M Charantimath, Entrepreneurship Development and Small Business Enterprises, Pearson Education, 2006.

Course Outcomes (COs):

At the end of the course, student will be able to

1. Plan and organize for the manpower in the given type of organization (PO-6, 8,10)
2. Use staffing Leading and controlling functions for the given organization. (PO-6, 7, 8, 9)
3. Analyze the advantages and potential drawbacks of Entrepreneurship. (PO-6, 7)
4. Develop a basic business plan and analyze the benefits of buying Franchise. (PO-3,5, 6, 7,10)
5. Identify the various institutions that provide financial support to small scale industries. (PO-6, 10)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30marks.		
Other components		
Quiz	10	CO1, CO2,CO3
Assignment	10	CO1, CO2, CO3, CO4, CO5
Semester End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5

EMBEDDED SYSTEM DESIGN	
Course Code: EC62	**Credits: 3:1:0**
Prerequisite: Microprocessor, EC44	**Contact Hours: 42L+28T**
Course Coordinator: Sara Mohan George, C Sharmila Suttur	

Course Contents

Unit I

Typical Embedded Systems: Core of the embedded system, memory, sensors and actuators, communication interface, other system components, characteristics and quality attributes of embedded systems

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Links: https://onlinecourses.nptel.ac.in/noc20_ee98/preview

Unit II

Programming for Embedded Systems: Overview of ANSI C, GNU development tools, bit manipulation using C, memory management, timing of programs, device drivers.
Types of files generated on cross compilation, disassembler/decompiler, simulators and emulators.
Hardware Software Co-Design and Program Modelling: Fundamental issues in hardware software co-design, computational models in embedded systems

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Links: https://onlinecourses.nptel.ac.in/noc23_cs54/preview

Unit III

GPIO and Interfacing: General purpose input/output ports, Interfacing of ADC, DAC, UART, I2C, LCD, stepper motor, LED, keypad and 7-segment display using data sheets of a microcontroller

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Links: https://onlinecourses.nptel.ac.in/noc22_cs93/preview

Unit IV

RTOS and IDE for Embedded System Design: Operating system basics, types of operating systems, tasks, Processes, Signals, process and threads, Multithreading, Multiprocessing and Multitasking, Task Scheduling: Scheduling Algorithms-Non Preemptive Scheduling, preemptive scheduling with numerical.

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Links: https://onlinecourses.nptel.ac.in/noc23_cs54/preview

Unit V

Inter-process communication: Task communication: Shared Memory, Pipes, Message Passing, Task Synchronization: task synchronization issues – racing and deadlock, Priority Inversion, Task Synchronisation Techniques: Semaphores-concept of binary and counting semaphores, how to choose an RTOS.

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Links: https://onlinecourses.nptel.ac.in/noc23_cs54/preview

TUTORIALS

1. Introduction to IAR Workbench / kiel
2. Introduction to C Programming, Programs in Embedded C
3. Programs to interface LEDS
4. Program to interface 7 segment displays
5. Program to interface Hex Keypad
6. Program to interface LCD
7. Program to interface ADC
8. Program to interface DAC
9. Introduction to LINUX
10. Keywords in LINUX
11. LINUX programming – Creation of process
12. LINUX programming - Signals
13. LINUX programming - multithreading
14. LINUX programming – semaphores

Text Books:

1. Dr. K. V. K. K. Prasad, "Embedded Real-Time Systems: Concepts, Design & Programming", Reprint Edition, Dreamtech Press, 2013.
2. Shibu K. V, "Introduction to Embedded Systems", 2nd Edition, Tata McGraw Hill Education, 2017.
3. James K. Peckol, "Embedded Systems – A Contemporary Design Tool", Student Edition, John Wiley and Sons, 2014.

References Books:

1. Steve Heath, "Embedded System Design", 2ndEdition, Newnes Publishers, 2003.
2. LPC 2148 user manual.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Identify the requirements of an embedded system (POs – 1, 3, PSO – 2)
2. Develop and debug embedded C programs (POs –1, 2, 3, 5, PSO – 2)
3. Design an embedded system using different peripherals (POs –2, 3, 4, 5, PSO – 2)
4. Illustrate RTOS concepts in embedded system design (POs –1, 2, 5, PSO – 2)
5. Demonstrate IPC with suitable C programs (POs – 1, 2, 5, PSO – 2)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1 & CO2
Internal test-II	30	CO3, CO4 & CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Assignment	10	C01, CO2, CO3
Quiz	10	CO1, CO2, CO3, CO4, CO5
Semester End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5

COMMUNICATION SYSTEMS LAB-II	
Course Code: ECL65	**Credits: 0:0:1**
Prerequisite: Communication Systems Lab-I	**Contact Hours: 28P**
Course Coordinator: Dr. C G Raghavendra	

Course Content

List of Experiments

1. Delta modulation and demodulation
2. Generation and detection of amplitude shift keying signals
3. Generation and detection of frequency shift keying signals
4. Generation and detection of phase shift keying signals
5. Generation and detection of quadrature PSK and DPSK
6. Simulation of line coding techniques
7. Simulation of ASK, FSK and PSK modulation techniques
8. Simulation of DPSK and QPSK modulation techniques
9. Simulation of Direct Sequence Spread Spectrum (DSSS) techniques.
10. Write a simulation code to analyze the performance of binary modulation schemes in the AWGN channel, and compare the results with theoretical results
11. Study of Huffman coding for encoding the source symbols

References Books:

1. J. G. Proakis and M. Salehi, "Contemporary Communication Systems Using MATLAB", PWS Publishing Company, 2007.
2. Simon Haykin, "Digital Communications", Wiley India Pvt. Ltd., 2006.
3. T.S. Rappaport, "Wireless Communications: Principles and Practice", 2nd Edition, Prentice Hall of India, Third Indian Reprint, 2010.

Web links and Video Lectures (e-Resources):

1. https://www.iitk.ac.in/mimt_lab/vlab/index.php
2. https://www.mathworks.com/help/comm/ug/bit-error-rate-analysis-techniques.html

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Implement delta modulation scheme (POs – 3, 4, 5, 7, 10, PSO – 3)
2. Implement ASK, PSK, FSK, DPSK digital modulation schemes (POs – 3, 4, 7, 10, PSO – 3)
3. Demonstrate the different line coding techniques and spread spectrum techniques (POs – 3, 4, 7, 10, PSO – 3)
4. Analyze the performance of the binary modulation techniques (POs – 3, 4, 7, 10, PSO – 3)
5. Demonstrate the role of source coding techniques in the end-to-end communication system (POs – 3, 4, 7, 10, PSO – 3)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Weekly evaluation of laboratory manuals/records after the conduction of every experiment	30	CO1, CO2, CO3, CO4, CO5
Practical test	20	CO1, CO2, CO3, CO4, CO5
Semester End Examination (SEE)	50	CO1, CO2, CO3, CO4, CO5

EMBEDDED SYSTEMS DESIGN LAB	
Course Code: ECL66	**Credits: 0:0:1**
Prerequisite: Microprocessor Lab	**Contact Hours: 28P**
Course Coordinator: C Sharmila Suttur	

Course Content

List of Experiments

Part A: RTOS Programs (System level programming by Linux API)

1. Creation of processes using fork()
2. Usage of "Signal" function calls–when DEL key or CTRL C is pressed, this sends a signal for abrupt termination
3. Multithreading – One thread reads the input from the keyboard and another thread converts to uppercase. This is done until 'Stop" is pressed. Number of threads can be running sharing same CPU.
4. Intertask communication using semaphore and pipes – Two threads, one for reading the input and one for converting the text to upper case letters, converting thread will wait for a semaphore to be released before it starts the operation and also pipes can be used to share the data from one thread to another
5. Intertask communication using mutex – Two threads, one for reading the input and one for converting the text to upper case letters, converting thread will wait for a semaphore to be released before it starts the operation and also pipes can be used to share the data from one thread to another
6. Interprocess communication using Message Queue – Reads the data from the queue and converts the text into upper case letters.
7. Use socket programming to create a server that continuously runs and sends the date and time as soon as a client connects to it and a client that will connect to the server and receive date and time from it.

Part B: Interface programs

1. Program to interface LCD and use SPI protocol for serial communication
2. Program to interface 7-segment and use I2C protocol for serial communication
3. Program to use ADC and display the variable voltage on LCD display
4. Waveform generation using the internal DAC of LPC2148
5. Program to monitor and control temperature using LPC2148

Text Books:

1. Dr. K. V. K. K. Prasad, "Embedded Real-Time Systems: Concepts, Design & Programming", Reprint Edition, Dreamtech Press, 2013.
2. Shibu K. V, "Introduction to Embedded Systems", 2nd Edition, Tata McGraw Hill Education, 2017.
3. James K. Peckol, "Embedded Systems – A Contemporary Design Tool", Student Edition, John Wiley and Sons, 2014.

References Books:

1. Steve Heath, "Embedded System Design", 2nd Edition, Newnes Publishers, 2003.
2. LPC 2148 user manual.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Develop embedded C programs (POs – 1, 2, 5, 8, 9, 11, PSO – 2)
2. Demonstrate embedded C programs to create process/tasks and threads for RTOS (POs – 1, 2, 5, 8, 9, 11, PSO – 2)
3. Illustrate inter-task communication using embedded C programs (POs – 1, 2, 5, 8, 9, 11, PSO – 2)
4. Design embedded C programs to interface data converters with a microcontroller (POs – 1, 2, 5, 8, 9, 11, PSO – 2)
5. Interface different types of I/O peripherals using a microcontroller for a typical application (POs – 1, 2, 5, 8, 9, 11, PSO – 2)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Weekly evaluation of laboratory manuals/records after the conduction of every experiment / Project	30	CO1, CO2, CO3, CO4, CO5
Practical test	20	CO1, CO2, CO3, CO4, CO5
Semester End Examination (SEE)	50	CO1, CO2, CO3, CO4, CO5

MINI PROJECT	
Course Code: EC67	**Credits: 0:0:4**
Prerequisite:	**Contact Hours: --**
Course Coordinator:	

EVALUATION RUBRICS FOR MINIPROJECT

Criteria	Max. Marks	Achievement Levels			Marks Awarded	CO Mapping
		Inadequate (0% - 33%)	**Development (34% - 66%)**	**Proficient (67% - 100%)**		
Introduction to Area & Problem Statement	**10**	No information about the specific technical details in the area	Some information about the area, but no clarity in internal details	Clear presentation of the technical working, and chosen area and rationale of design choices		**CO1**
Explanation of Technical Block Diagram	**10**	Block diagram is technically incorrect or is not practical	Technically correct block diagram but not feasible in practical settings	Technical correct block diagram with tools and resources for implementation available		**CO2**
Implementation of Block Diagram	**10**	Incomplete implementation of block diagram	Block diagram is implemented but results not generated	Block diagram is complete, with results matching reference works		**CO3**
Results & Discussion	**10**	No results and no functionality generated	Results generated, but not in a comprehensive manner	Results generated along with Design of Experiments for comprehensive testing		**CO4**
Report Writing	**10**	Proper technical language not used	Proper technical language along with flow from beginning to end	Technical language, flow, and graphical elements used extensively to express hypotheses		**CO5**

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Demonstrate a basic knowledge in the chosen domain (POs – 1, 2, 3, 4, 6,7, 8, 9, 10, 11, PSO – 1)
2. Describe concepts in an accurate manner (POs – 2, 3, 7, 8, 9, 10, PSOs – 2, 3)
3. Discuss technical issues in the chosen domain (POs – 2, 3, 4, 5, 6,7 ,8, 9, 10 PSOs – 2, 3)
4. Propose technical solutions to practical problems/bottleneck in the chosen domain (POs –1 2, 3, 4, 5, 6, 7, 8 , 9, 11, PSOs – 2, 3)
5. Create a technical document expressing the details of work done (POs – 7, 8, 9,11, PSOs – 2, 3)

Technical Skill Enhancement Course	
Course Code: ECAEC691	**Credits: 0:1:0**
Prerequisite: --	**Contact Hours: 28T**
Course Coordinator: Raghuram S	

Course Contents

1. Circuit Theory & Network Analysis
2. Analog Electronic Circuits
3. Digital Electronic Circuits (Combinational)
4. Digital Electronic Circuits (Sequential)
5. Signals & Systems
6. Digital Signal Processing
7. Microwaves & Antennas
8. Communication Systems – I
9. Communication Systems – II
10. Embedded Systems Design
11. CMOS VLSI Design – I
12. CMOS VLSI Design – II
13. Mock Interviews
14. Mock Interviews

Industry experts in relevant domains will be invited to deliver lectures on practical aspects of these topics to the students.

Course Outcomes (COs)

CO1: Analyze performance parameters of analog circuit designs keeping in mind practical issues in design (PO-1, 2, 3, 4, 11)
CO2: Design circuits that can be used in practical digital designs. (PO-1, 2, 3, 4, 11)
CO3: Apply fundamental knowledge in the signal and systems and DSP domains in practical applications (PO-1, 2, 3, 4, 11)
CO4: Analyze communication systems from a practical perspective (PO-1, 2, 3, 4, 11)
CO5: Design and develop VLSI circuits and systems keeping in mind practical constraints (PO-1, 2, 3, 4,11)

VI Semester Electives

DIGITAL VLSI TESTING	
Course Code: ECE631	**Credits: 3:0:0**
Prerequisite: Digital Design, CMOS VLSI Design	**Contact Hours: 42L**
Course Coordinator: Parameshwara M C	

Course Contents

Unit I

Introduction: Role of testing, Testing during the VLSI life cycle, Challenges in VLSI testing, test economics, Yield, Fault coverage

Fault Modeling: Various fault models, Single Stuck-at fault – fault equivalence, fault collapsing.

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Links: https://nptel.ac.in/courses/117105137
  https://drive.google.com/file/d/1n6agUcye7HE1xPItwQ03wow0b3g6NloU/view

Unit II

Logic and Fault Simulation: Simulation Models, Algorithms for true value simulation, Algorithms for fault simulation, Statistical methods for fault simulation.

Testability Measures: Controllability and Observability, SCOAP Testability analysis.

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Links: https://nptel.ac.in/courses/117105137
  https://drive.google.com/file/d/1n6agUcye7HE1xPItwQ03wow0b3g6NloU/view

Unit III

Combinational Circuit Test Generation: ATPG Algebras, Combinational ATPG Algorithms – D-Algorithm, PODEM, FAN.

DFT and Scan Design: Ad-Hoc DFT, Scan based design.

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Links: https://nptel.ac.in/courses/117105137
  https://drive.google.com/file/d/1n6agUcye7HE1xPItwQ03wow0b3g6NloU/view

Unit IV

Sequential Circuit Test Generation: Time frame expansion method, Simulation-based sequential ATPG.

Logic BIST: Test pattern generation, output response analyzer, BIST architectures, Fault coverage enhancement.

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Link: https://nptel.ac.in/courses/117105137
  https://drive.google.com/file/d/1n6agUcye7HE1xPItwQ03wow0b3g6NloU/view

Unit V

Boundary Scan: Introduction and motivation, TAP controller and port, SOC test problems.

Memory Test: Notation, Faults – Fault Manifestations, Failure Mechanisms, Memory Test Levels, March Test Notation, Fault Modeling – Diagnosis Versus Testing Needs, Reduced Functional Faults

- Pedagogy/Course delivery tools: Chalk and talk, power point presentations
- Links: https://nptel.ac.in/courses/117105137
  https://drive.google.com/file/d/1n6agUcye7HE1xPItwQ03wow0b3g6NloU/view

Text Books:

1. Laung-Terng Wang, Cheng-Wen Wu andXiaoqing Wen, (Eds.), "VLSI Test Principles and Architectures: Design for Testability", Morgan Kaufmann Publishers, 2006.
2. Michael L. Bushnell, Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002.

References Books:

1. Zainalabedin Navabi, "Digital System Test and Testable Design", Springer New York, NY, 2011
2. Parag K. Lala, "Digital Circuit Testing and Testability", Academic Press, 1997

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Create and manipulate fault models of VLSI circuits. (POs – 1, 3, 4)
2. Perform fault simulations, and predict testability measures of digital circuits. (POs – 1, 3, 4)
3. Generate optimized test patterns for combinational and sequential logic circuits. (POs – 1, 3, 4)
4. Design scan chains and BIST modules for digital designs. (POs – 1, 3, 4)
5. Employ boundary scan elements in design. (POs – 1, 3, 4)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Seminar	10	CO1, CO2, CO3
Virtual lab/ Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

INFORMATION THEORY AND CODING	
Course Code: ECE632	**Credits: 3:0:0**
Prerequisite: Engineering Maths	**Contact Hours: 42L**
Course Coordinator: V Nuthan Prasad	

Course Contents

Unit I

Introduction to Information Theory: Measure of information theory, Average information content of symbols in long independent sequence, Dependent source, Independent source

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117101053

Unit II

Source Coding: Huffman coding, Arithmetic Coding, LZW Algorithm, Run Length Coding

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117101053

Unit III

Discrete Communication Channels: Communication Channels, Channel Models, Channel Matrix, Joint Probability Matrix, Mutual Information, Channel Capacity, Special Channel, Capacity of: Binary Symmetric Channel, Binary Erasure Channel, Muroga's Theorem.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117101053

Unit IV

Error Control Coding: Introduction, Linear Block Codes: matrix description of Linear Block Codes, Error Detection and Error Correction Capabilities of Linear Block Codes, Single Error Correcting Hamming Codes, Table lookup Decoding-using Standard Array.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117101053

Unit V

Binary Cyclic Codes and Convolution Codes: Algebraic Structure of Cyclic Codes, Encoding using an (n-k) Bit-Shift register, Syndrome Calculation, Error Detection and Correction, Convolution Encoder, Time domain approach, Transform domain approach, code Tree, Trellis and State Diagram.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117101053

Text Books:

1. K. Sam Shanmugham, "Digital and analog communication Systems", John Wiley Publications, 1996.
2. Shu Lin, Daniel J. Costello, "Error Control Coding", 2nd Edition Pearson / Prentice Hall, 2004.
3. Simon Haykin, "Digital Communications", 2nd Edition, John Wiley Publications, 2015

References Books:

1. Bernard Sklar, "Digital Communications", Pearson Education, 2015
2. Simon Haykin, "Introduction to Analog and Digital Communications", John Wiley Publications, 2012

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Apply the basics of information theory to compute entropy and information rate. (POs-1,2,3,4 PSO-3)
2. Design various coding techniques. (POs-1,2,3,4 PSO-3)
3. Categorize various channels for information transmission and interpret Shannon's theorem in continuous channels. (POs-2,3,4 PSO-3)
4. Design Linear Block Codes in error detection and error correction. (POs-2,3,4 PSO-2,3)
5. Model Cyclic Block Codes and Construct trellis diagrams for Convolution encoders. (POs-2,3,4,5 PSO-2,3)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1 & CO2
Internal test-II	30	CO3, CO4 & CO5
The average of the two internal tests shall be taken for 30 marks.		
Other components		
	20	CO1, CO2, CO3, CO4 & CO5
Semester-End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5

IMAGE AND VIDEO PROCESSING	
Course Code: ECE633	**Credits: 3:0:0**
Prerequisite: Signal Processing	**Contact Hours: 42L**
Course Coordinator: Mamtha Mohan	

Course Contents

Unit I

Fundamentals: Introduction to Digital Image Processing, Image sensing and acquisition, Image sampling and quantization, Some basic relationship between pixels, Mathematical tools in Digital Image processing

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117105135

Unit II

Intensity Transformations and Spatial Filtering: Basics of intensity transformations and spatial filtering, Basic intensity transformation functions, Histogram processing, Mechanics of spatial Filtering, Smoothing and Sharpening spatial filters

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117105135

Unit III

Image Transforms: 1D and 2D Discrete Fourier Transform pair (DFT), properties of 2D DFT
Filtering in Frequency Domain: Basics of filtering in frequency domain, Image smoothing using low pass frequency domain filters – Ideal, Gaussian, and Butterworth low pass filters, Image sharpening using high pass filters – Ideal, Gaussian, and Butterworth high pass filters

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/117105135

Unit IV

Digital Video: Spatial resolution and frame rate, color image processing, digital video standards.
3 D video: 3D-Display Technologies Stereoscopic Video, Multi-View Video
Digital-Video Applications: Digital TV, Digital Cinema, Video Streaming over the Internet Computer Vision and Scene/Activity Understanding

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://archive.nptel.ac.in/courses/117/104/117104020/

Unit V

Two-Dimensional Motion Estimation: Optical flow, General Methodologies, Pixel-Based Motion Estimation, Block-Matching Algorithm

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://archive.nptel.ac.in/courses/117/104/117104020/

Text Books:

1. R C. Gonzalez, R.E. Woods, "Digital Image Processing", 4th Edition, Pearson Education 2018.
2. Murat Tekalp, "Digital Video Processing", 2nd Edition, Pearson Education, Inc, 2010.

References Books:

1. R. C. Gonzalez, R. E. Woods, S. L. Eddins, "Digital Image Processing using MATLAB", 2nd Edition, Pearson Education, 2017.
2. Anil. K. Jain, "Fundamentals of Digital Image Processing", Prentice Education, 2002.
3. Yao wang, Joem Ostarmann and Ya – quin Zhang, "Video processing and communication" 1st edition , PHI,2002

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Analyze general terminology of digital image processing and employ basic intensity transformation functions. (POs – 1, 2, 3, 5, PSO – 3)
2. Interpret smoothing and sharpening of images using frequency domain filters and appreciate various image transforms. (POs – 2, 3, 5, PSO – 3)
3. Evaluate the methodologies for segmentation and classification of objects in an image. (POs – 1, 2, 3, 5, PSO – 3)
4. Appraise different models for video processing and motion estimation. (POs – 1, 2, 3, 5, PSO – 3)
5. Apply video processing techniques in practical applications. (POs – 1, 2, 3, 5, PSO – 3)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Virtual lab/ Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5

ROBOTICS	
Course Code: ECE634	**Credits: 3:0:0**
Prerequisite: Nil	**Contact Hours: 42L**
Course Coordinator: Lakshmi Shrinivasan	

Course Contents

Unit I

Basic Concepts: Definition of robotics, Robotic architecture, Classification of robots, Industrial applications

Actuators and Grippers: Electric actuator, Hydraulic, Pneumatic, Electric drives

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/112105249
  https://nptel.ac.in/courses/112101099

Unit II

Internal and External Sensors: Internal sensors, Position sensors, Incremental encoder, Absolute encoder, Resolver velocity sensors, Tachometer and hall effect sensor, Acceleration and forces sensors, Hall effect, Touch sensors, Proximity sensors, Ultrasonic sensors, Laser sensors for range measurements, Machine vision sensors

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/112105249
  https://nptel.ac.in/courses/112101099

Unit III

Transformation: Rotation matrix, Composite rotation matrix, Rotation matrix with Euler angles representation, Homogenous transformation matrix, DH representation, Homogenous transformation for various arm configurations

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/112105249
  https://nptel.ac.in/courses/112101099

Unit IV

Robotic Operating System (ROS): Introduction to ROS, OpenCV, OpenNI, PCL – Programming Kinect with Python using ROS, OpenCV, OpenNI– Point clouds using Kinect, ROS, OpenNI, PCL

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://www.youtube.com/watch?v=0BxVPCInS3M
  https://nptel.ac.in/courses/112105249

Unit V

Interfacing with ROS: Building ChefBot hardware, ROS Python driver for ChefBot, ChefBot ROS launch files, ChefBot Python nodes and launch files, Calibration and testing of ChefBot

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://chefbotbuild.wordpress.com
  https://nptel.ac.in/courses/112101099

Text Books:

1. S K Saha, "Introduction to Robotics", 2nd Edition, McGraw Hill Education Pvt. Ltd, 2008.
2. S Fu, R C Gonzalez, C S G Lee, "Robotics Control, Sensing Vision and Intelligence", 3rd Edition, McGraw Hill International, 2016.
3. Lentin Joseph, "Learning Robotics using Python", 2ndEdition, PACKT Publishing, 2015.

References Books:

1. Mikell P, Weiss G M, Nagel R N, "Industrial Robotics: Technology, Programming, and Applications", 2nd Edition, McGraw Hill International, 2012.
2. Martinez, E. Fernandez, "Learning ROS for Robotics Programming", PACKT Publishing, 2013.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Appreciate the architecture and applications of robots (POs – 1, 2, 3, PSO – 1)
2. Analyze the principles of various sensors and their applications in robots (POs – 1, 2, 3, PSO – 1)
3. Apply DH parameter and homogenous transforms for robotic applications (POs –1, 2, 3, 5, PSO – 1)
4. Acquire the knowledge of ROS. (PO – 1, 2, 3, PSO – 1)
5. Describe hardware design of ChefBot. (PO – 1, 2, 3, 4, 5, PSO – 1)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Mini-project/Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5

MIXED SIGNAL IC DESIGN	
Course Code: ECE641	**Credits: 3:0:0**
Prerequisite: Analog Circuits	**Contact Hours: 42L**
Course Coordinator: M Nagabushanam	

Course Contents

Unit I

Introduction and Single Stage Amplifiers: MOS device basics, MOS device models, Common Source Amplifiers, Source Follower, Common Gate, Cascode Structures, and Folded Cascode Structures

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/108106105

Unit II

Differential Amplifier and Current Mirrors: Introduction to Differential Pair Amplifier, Quantitative Analysis to Differential Pair Amplifier, Common Mode Response, Differential Amplifiers with Different Loads, Effects of mismatches. Simple Current Mirrors, Cascode Current Mirrors, Differential Pair with Current Mirror Load

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/108106105

Unit III

Operational Amplifiers: Op Amps Low-Frequency Analysis, Telescopic Op-Amps, Folded Cascode Op-Amps, Two-Stage Op-Amps, Common Mode Feedback, Cascode Structures and Folded Cascode Structures.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/108106105

Unit IV

Data Converter Fundamentals: Analog versus Discrete-Time Signals, Converting Analog Signals to Digital Signals, Sample-and-Hold Characteristics, Digital-to-Analog Converter Specifications, Analog-to-Digital Converter Specifications.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://www.youtube.com/watch?v=xdoAB7jevk0

Unit V

DAC and ADC Architectures: Digital Input Code, Resistor String, R-2R Ladder Networks, Pipeline DAC, ADC Architectures: Two-Step Flash ADC, Pipeline ADC, Successive Approximation ADC

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://www.youtube.com/watch?v=kMGap-0XwGs&t=13s
  https://www.youtube.com/watch?v=LUMhObAm1Qs

Text Books:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Education (India) Edition, 2018.
2. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, John Wiley & Sons. Inc., Publishing, 2010

References Books:

1. P E Allen and D R Holberg, "CMOS Analog Circuit Design", 2nd Edition, Oxford University Press, 2002.
2. Behzad Razavi, "Fundamentals of Microelectronics", 1st Edition, Wiley Publishing, 2008.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Employ the concept of MOS devices in various MOS amplifier configurations (POs – 1, 2, 3, 4, 7,11, PSO – 2)
2. Design differential amplifiers with different MOS loads. (POs – 1, 2, 3, 4, 7, 11 PSO – 2)
3. Construct one/two-stage op-amp and analyze the frequency response of op-amps. (POs – 2, 3, 4, PSO – 2)
4. Define various specifications of ADCs/DACs (POs – 2, 3, 4, 7, PSO – 2)
5. Illustrate different types of ADC and DAC architectures (POs – 2, 3, 4, 7, PSO – 2)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5

COMPUTER ARCHITECTURE	
Course Code: ECE642	**Credits: 3:0:0**
Prerequisite:	**Contact Hours: 42L**
Course Coordinator: V Anandi	

Course Contents

Unit I

Introduction: Combinational and Sequential Logic Circuits, Computer Systems, Uniprocessors & Multiprocessors

Instruction Sets: Computer Hardware, Representing Instructions in the Computer, Instructions for Making Decisions, and Sample Instruction Sets.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106106134

Unit II

Computer Arithmetic: Addition and Subtraction, Multiplication, Division, Floating Point Parallelism, and Computer Arithmetic

The Processor: Introduction, Logic Design Conventions, Building a Datapath, A Simple Implementation Scheme, Overview of Pipelining, Pipelined Datapath, Hazards, Exceptions

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106106134

Unit III

Memory Hierarchy: Introduction, Memory Technologies, Basics of Caches Measuring and Improving Cache Performance, Memory Hierarchy, Virtual Machines Virtual Memory.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106106134

Unit IV

Parallel Processors from Client to Cloud: Introduction, Parallel Processing Programs, SISD, MIMD, SIMD, SPMD, Vector, Hardware Multithreading, Multicore and Other Shared Memory Multiprocessors

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106106134

Unit V

Graphics and Computing GPUs: Introduction, GPU System Architectures, Programming GPUs, Multithreaded Multiprocessor Architecture, Parallel Memory System, NVIDIA GeForce 8800 B-46, Mapping Applications to GPUs

- Pedagogy/Course delivery tools: Chalk and talk

Text Books:

1. David A Patterson, John L Hennessey, "Computer Organization and Design: The Hardware Software Interface, The Morgan Kaufmann [RISC-V Edition] 2017.

References Books:

1. Kai Hwang and Zu, "Scalable Parallel Computers Architecture" Tata McGraw Hill, 1st Edition, 2003
2. D.A. Patterson, J.L. Hennessy, "Computer Architecture: A quantitative approach" 5th Edition, Morgan Kaufmann, 2012.

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Discuss contemporary computer architecture issues and techniques. (POs – 1,2,6 PSO - 2)
2. Design basic and intermediate RISC pipelines. (POs - 2,3,4,12 PSO - 2)
3. Discuss hierarchical memory organization of a system (POs - 1,2,3,5 PSO - 2)
4. Compare properties of shared memory and distributed multiprocessor systems. (POs - 2,3,6 PSO - 2)
5. Explain multithreading architectures and GPU. (POs - 2,3,6 PSO - 2)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1, CO2, CO3
Internal test-II	30	CO3, CO4, CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz	10	CO1, CO2, CO3
Assignment	10	CO3, CO4, CO5
Semester End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5

CRYPTOGRAPHY AND NETWORK SECURITY	
Course Code: ECE642	**Credits: 3:0:0**
Prerequisite: Nil	**Contact Hours: 42L**
Course Coordinator: Chitra M	

Course Contents

Unit I

Basic Concepts of Number Theory and Finite Fields: Divisibility and the divisibility algorithm, Euclidean algorithm, Modular arithmetic, Groups, Finite fields of the form GF(p), Polynomial arithmetic, Finite fields of the form GF(2n), Prime Numbers, Fermat's and Euler's theorem, Primality testing, Chinese Remainder Theorem, Discrete logarithm.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106105031

Unit II

Classical Encryption Techniques: Symmetric cipher model, Substitution techniques, Steganography.

Symmetric Ciphers: Data encryption standard (DES), The AES Cipher.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106105031

Unit III

Principles of Public-Key Cryptosystems: The RSA algorithm, Diffie - Hellman Key Exchange, ElGamal Cryptosystem, Elliptic Curve Arithmetic, Elliptic Curve Cryptography.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106105031

Unit IV

Cryptographic Data Integrity Algorithms and Network Security: Applications of cryptographic hash functions, Message authentication requirements and functions, Message authentication codes, Security of hash functions and codes.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106105031

Unit V

Network Security Applications: Authentication Applications- Kerberos Version 5, X.509 Authentication Service, Public Key Infrastructure; Electronic Mail Security-Pretty Good Privacy, S/MIME; IP Security.

- Pedagogy/Course delivery tools: Chalk and talk
- Links: https://nptel.ac.in/courses/106105031

Text Books:

1. W. Stallings, "Cryptography and Network Security", 7th Edition, Pearson Education, 2017.
2. Atul Kahate, "Cryptography and Network Security", 3rd Edition, TMH, 2017.

References Books:

1. Forouzan, "Cryptography & Network Security", 2nd Edition, Tata McGraw Hill, 2010

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Use basic cryptographic algorithms to encrypt the data. (POs – 1, 2, PSOs – 1, 3)
2. Demonstrate the different encryption techniques, design principles and modes of operation. (POs – 1, 2, PSOs – 1, 3)
3. Apply symmetric cipher for digital data. (POs – 1, 2, 3, PSOs – 1, 3)
4. Examine various network security algorithms. (POs – 1, 2, 3, 4, PSOs – 1, 3)
5. Summarize various Network security applications. (POs – 1, 2 PSOs – 1, 3)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1 & CO2
Internal test-II	30	CO3, CO4 & CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Quiz/Assignment	20	CO1, CO2, CO3, CO4 & CO5
Semester End Examination (SEE):	100	CO1, CO2, CO3, CO4, CO5

MACHINE LEARNING AND DEEP LEARNING	
Course Code: ECE 644	**Credits: 3:0:0**
Prerequisite: Probability & Linear Algebra	**Contact Hours: 42L**
Course Coordinator: Raghuram S	

Course Contents

Unit I

Introduction: Example machine learning applications

Perceptron Algorithm: Training a perceptron, Learning Boolean functions, Multilayer perceptrons

Supervised Learning: Noise, Learning multiple classes, Regression, Model selection, and generalization

Bayesian Decision Theory: Classification, Losses and Risks, Discriminant functions, Association Rules

- Pedagogy/Course delivery tools: Chalk and talk PPT
- Link: https://onlinecourses.nptel.ac.in/noc23_cs18/preview

Unit II

Parametric Methods: Maximum likelihood estimation, Evaluating an estimator, Bayes estimator, Parametric classification, Regression, Tuning model capacity

Dimensionality Reduction: Subset Selection, Principal Component Analysis (PCA), SVD and Matrix factorization, Linear Discriminant Analysis (LDA)

Decision Trees: Univariate and Multivariate trees

- Pedagogy/Course delivery tools: Chalk and talk PPT
- Link: https://onlinecourses.nptel.ac.in/noc23_cs18/preview

Unit III

Unsupervised Learning: Clustering: k–Means Clustering, EM algorithm, Hierarchical Clustering

Support Vector Machines: Kernels, Geometric Margins, SVM: Primal and dual forms, Kernelizing SVM

- Pedagogy/Course delivery tools: Chalk and talk PPT
- Link: https://onlinecourses.nptel.ac.in/noc23_cs18/preview

Unit IV

Deep feedforward networks: Learning XOR, Gradient Based Learning, Hidden Units, Architecture Design, Backpropagation Algorithm

Convolutional Neural Networks: Convolution operation, pooling, Variations of convolution function, convolution algorithm

- Pedagogy/Course delivery tools: Chalk and talk PPT
- Link: https://onlinecourses.nptel.ac.in/noc23_cs18/preview

Unit V

Regularization for Deep Learning: Parameter Norm Penalties, Dataset Augmentation, Early Stopping, Bagging, Dropout, Adversarial Training

Boosting: Boosting Accuracy, Adaboost

Sequence Modeling: Recurrent and Recursive nets, LSTM, Gated RNNs, Practical methodology, Applications

- Pedagogy/Course delivery tools: Chalk and talk PPT
- Link: https://onlinecourses.nptel.ac.in/noc23_cs18/preview

Text Books:

1. Ethem Alpaydin, "Introduction to Machine Learning", 3rd Edition, PHI Learning Pvt. Ltd, 2015.
2. Ian Goodfellow, Yoshua Bengio, Aaron Courville, "Deep Learning", MIT Press, 2017

References Books:

1. Christopher Bishop, "Pattern Recognition and Machine Learning", CBS Publishers & Distributors, 2010.
2. Tom Mitchell, "Machine Learning", McGraw Hill, 1997.
3. Michael Nielsen, "Neural Networks and Deep Learning", 2019

Course Outcomes (COs):

At the end of the course, students will be able to:

1. Examine the concepts of various supervised learning algorithms, basics of perceptron's and employ Bayesian learning for classification. (POs – 1, 2,3,4, PSOs – 3)
2. Evaluate parametric methods for classification and investigate various dimensionality reduction algorithms (POs – 1, 2,3,4, PSOs – 3)
3. Analyse unsupervised learning, multivariate concepts and SVM (POs – 1, 2, 3,4, PSOs – 3)
4. Appreciate the concepts of deep learning and apply deep feed forward network practical problem. (POs – 2, 3, 4,5, PSOs - 3)
5. Apply convolutional networks and demonstrate functioning of recurrent and recursive neural networks (POs – 2,3,4,5, PSOs – 3)

Course Assessment and Evaluation:

Continuous Internal Evaluation (CIE): 50 Marks		
Assessment Tool	**Marks**	**Course outcomes addressed**
Internal test-I	30	CO1 & CO2
Internal test-II	30	CO3, CO4 & CO5
Average of the two internal tests shall be taken for 30 marks.		
Other components		
Mini-Project	20	CO1, CO2, CO3, CO4 & CO5
Semester End Examination (SEE)	100	CO1, CO2, CO3, CO4, CO5